

PG180-A02

256b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

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Page Description

51	SEQUENCE: MISC
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base on V372-02S change for D18 Z
1. P.23 remove SL1 & BRIDGE_LED_VDD & SL1_BRG_PRST*
2. P.52 remove LED change FAN connector
3. P.53 remove LED
4. P.38/44 add FUSE
5. P.5~14 mem add <->
6. P.53 LED use V336-0D
7. P.32 remove
8. P.35~38 dual MOS
9. P.33 change dual MOS
10. P.43 remove
11. P.31 change to UP1666
12. P.21 remove colay DP

0727:

page 24: REMOVE GPIO29_IDLE_IN_SW
remove GPIO9_INPUT_DYN_BAL2
page 29: 12V_F RTD3 change to 12V_F
page 30: 12V_F RTD3 change to 12V_F
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移除保護線路
page 39: remove INPUT SWITCH RTD3
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page 44: remove INA3221

page 46: remove PFM_SKIP net
remove PS_RTD3_12V_SW net
page 47: remove PS_VMON_PGOOD net
12V_F RTD3 change to 12V_F
remove 3V3_PORT
remove 3V3_RTD3 change to nv3v3
page 48: remove OC_CRIT* NET from ina3221
remove PS_VMON_PGOOD net
page 49: PCIE Voltage Monitor1
page 52: REMOVE VIN =>12V_PEX6_8_IN_OVRS

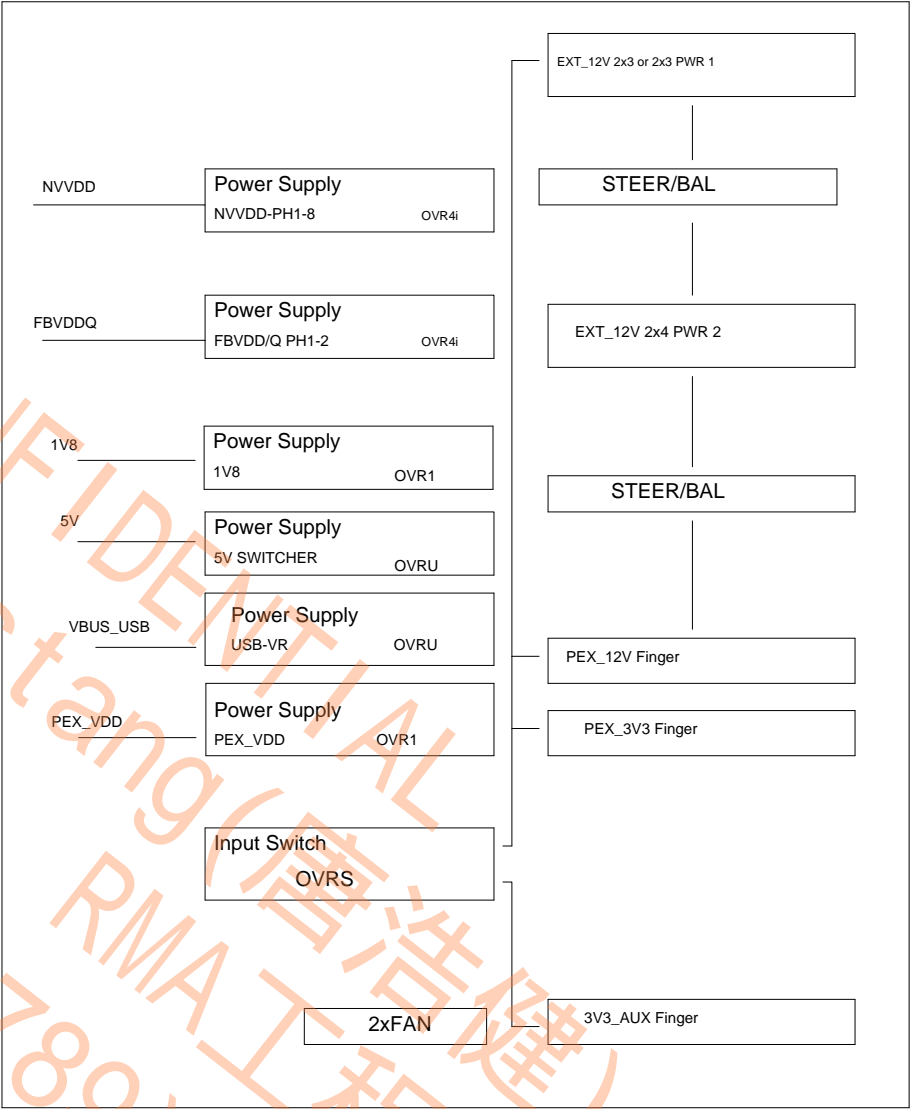
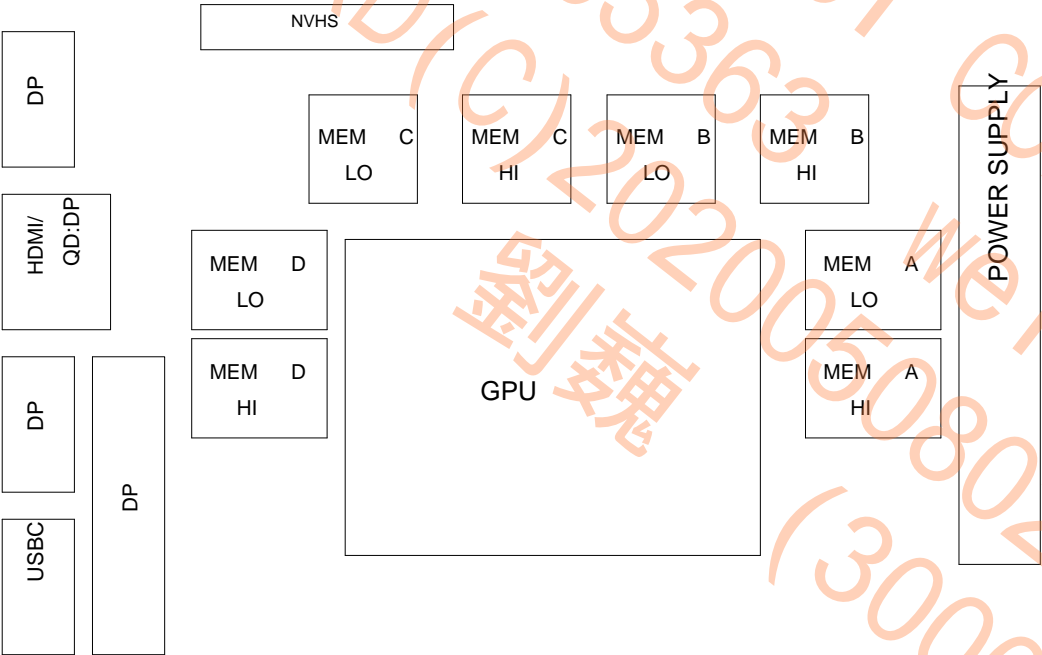
page 54: change GPU screw holes to small size

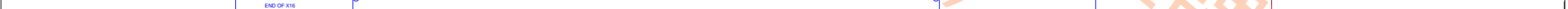


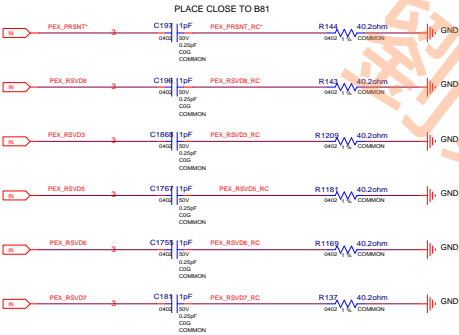
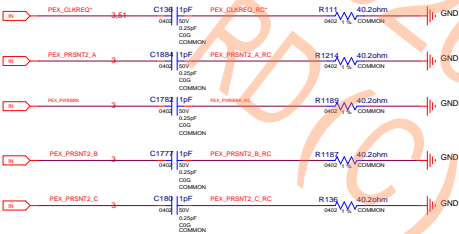
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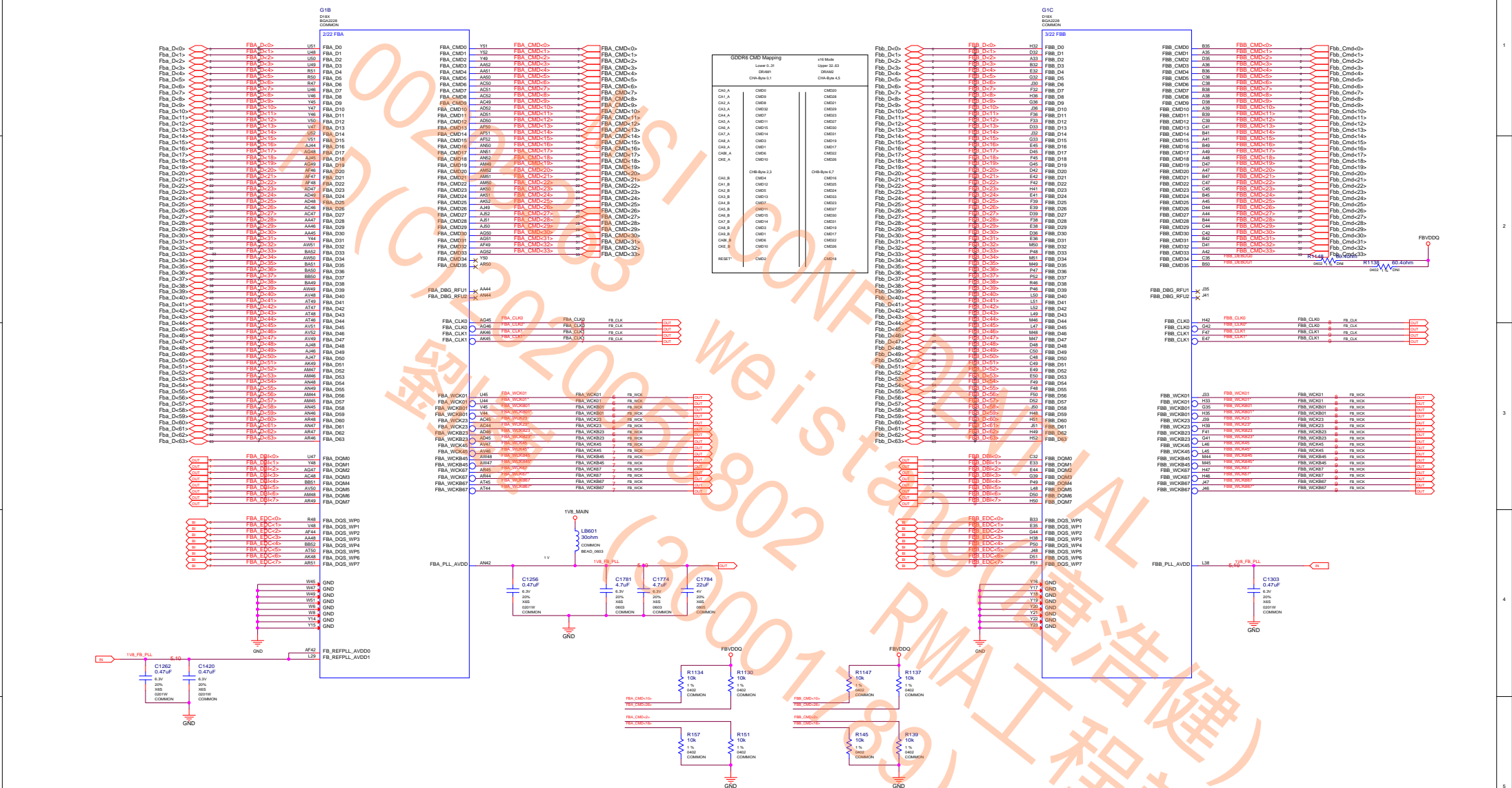
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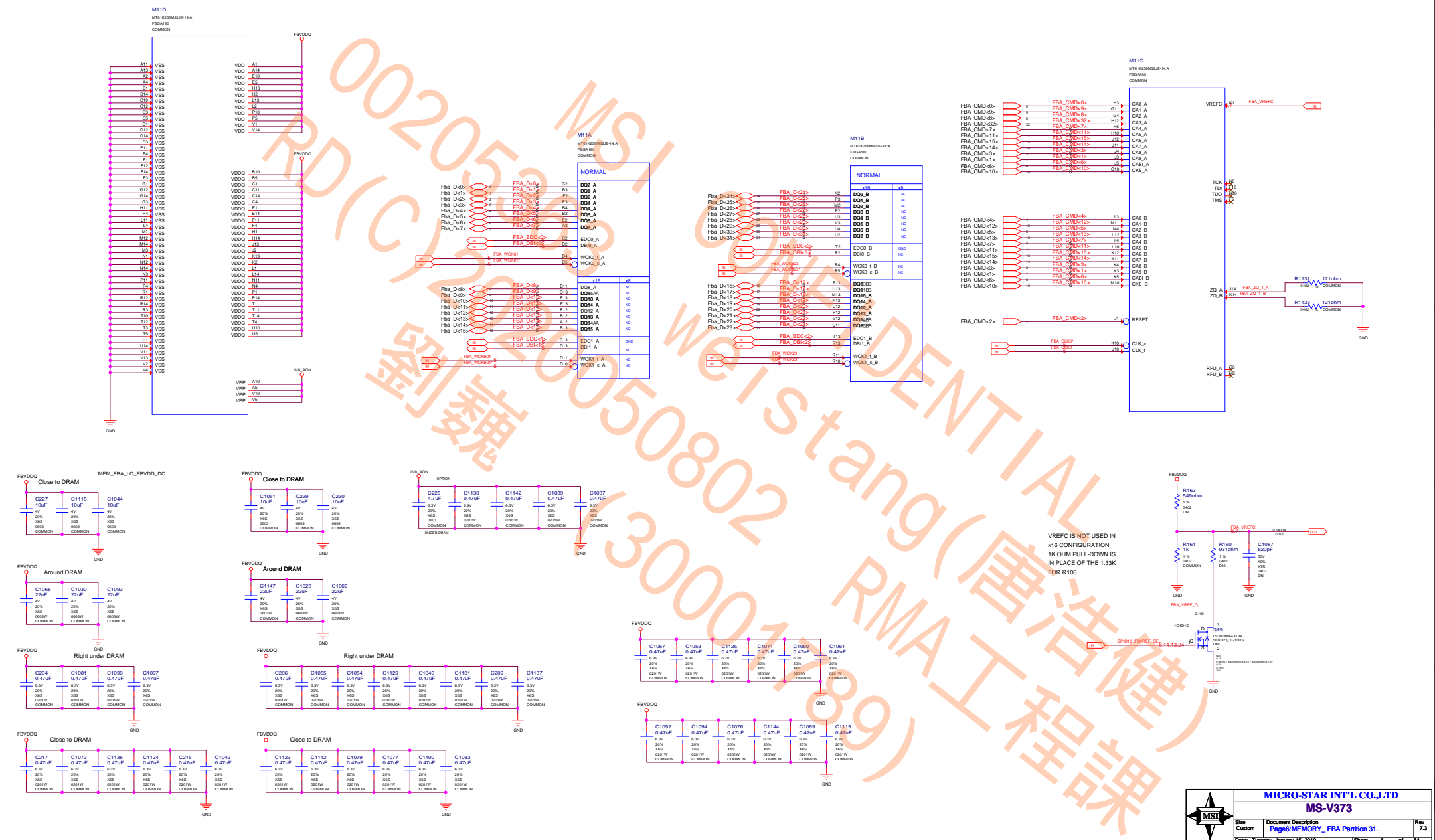
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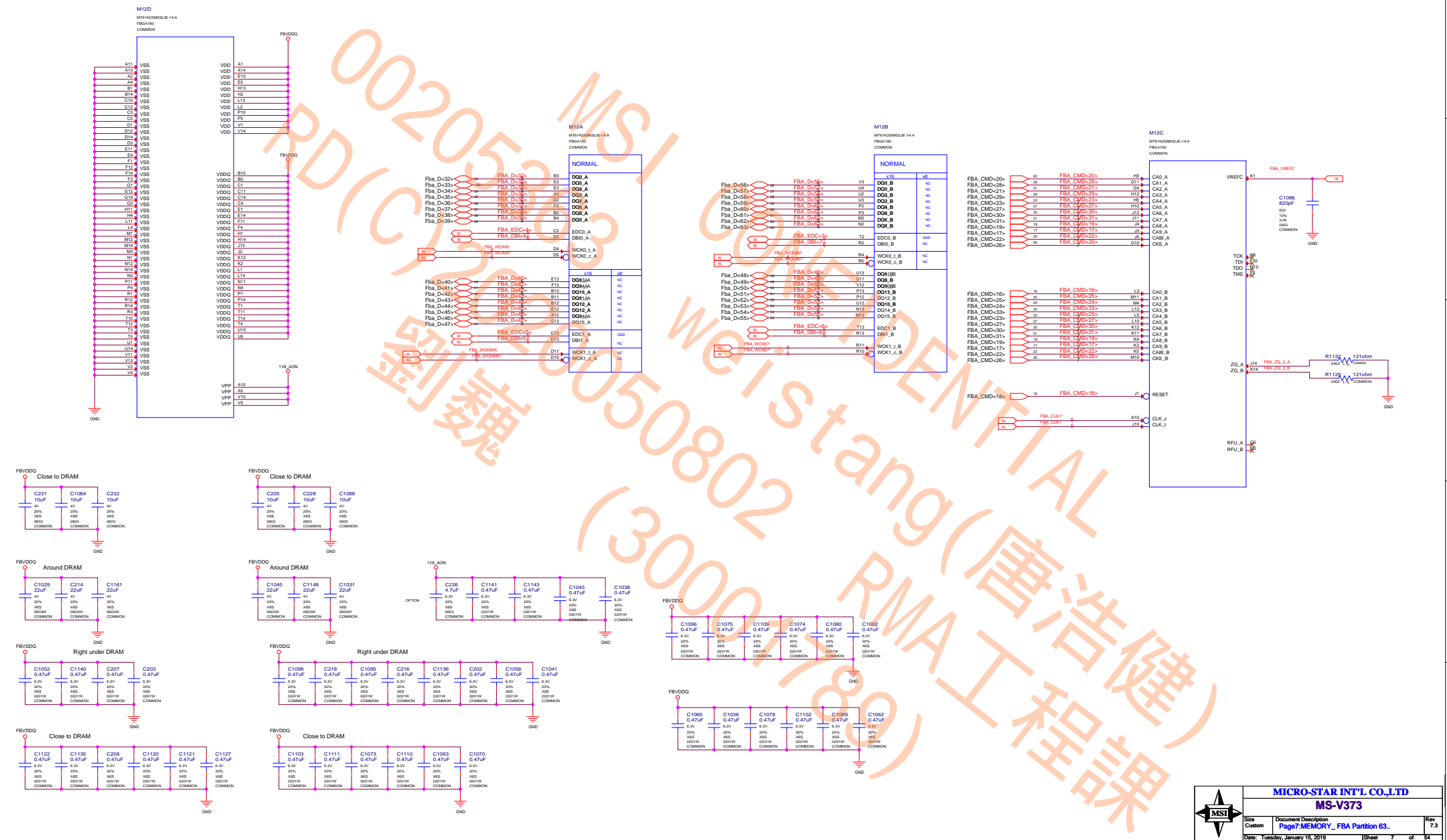


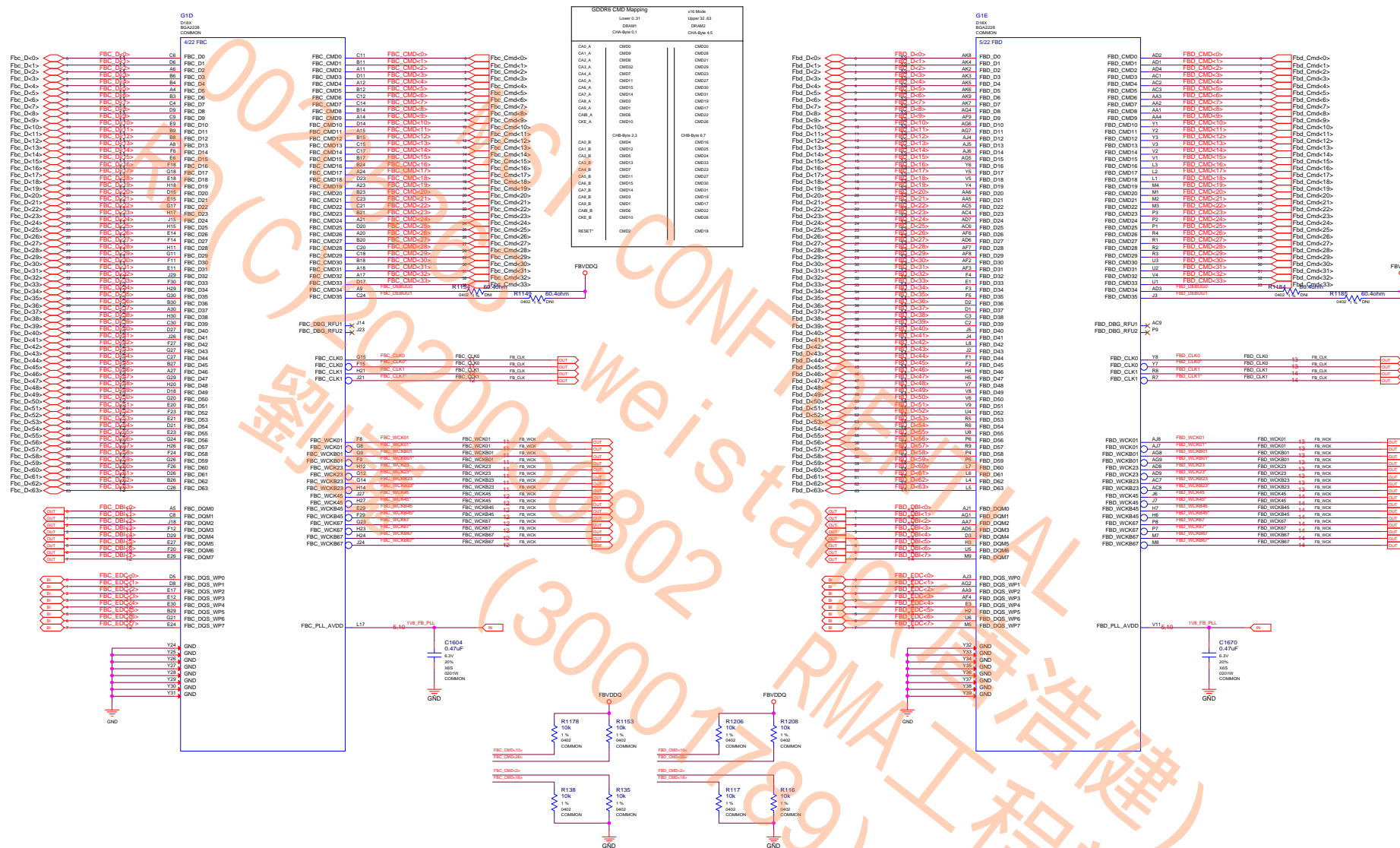


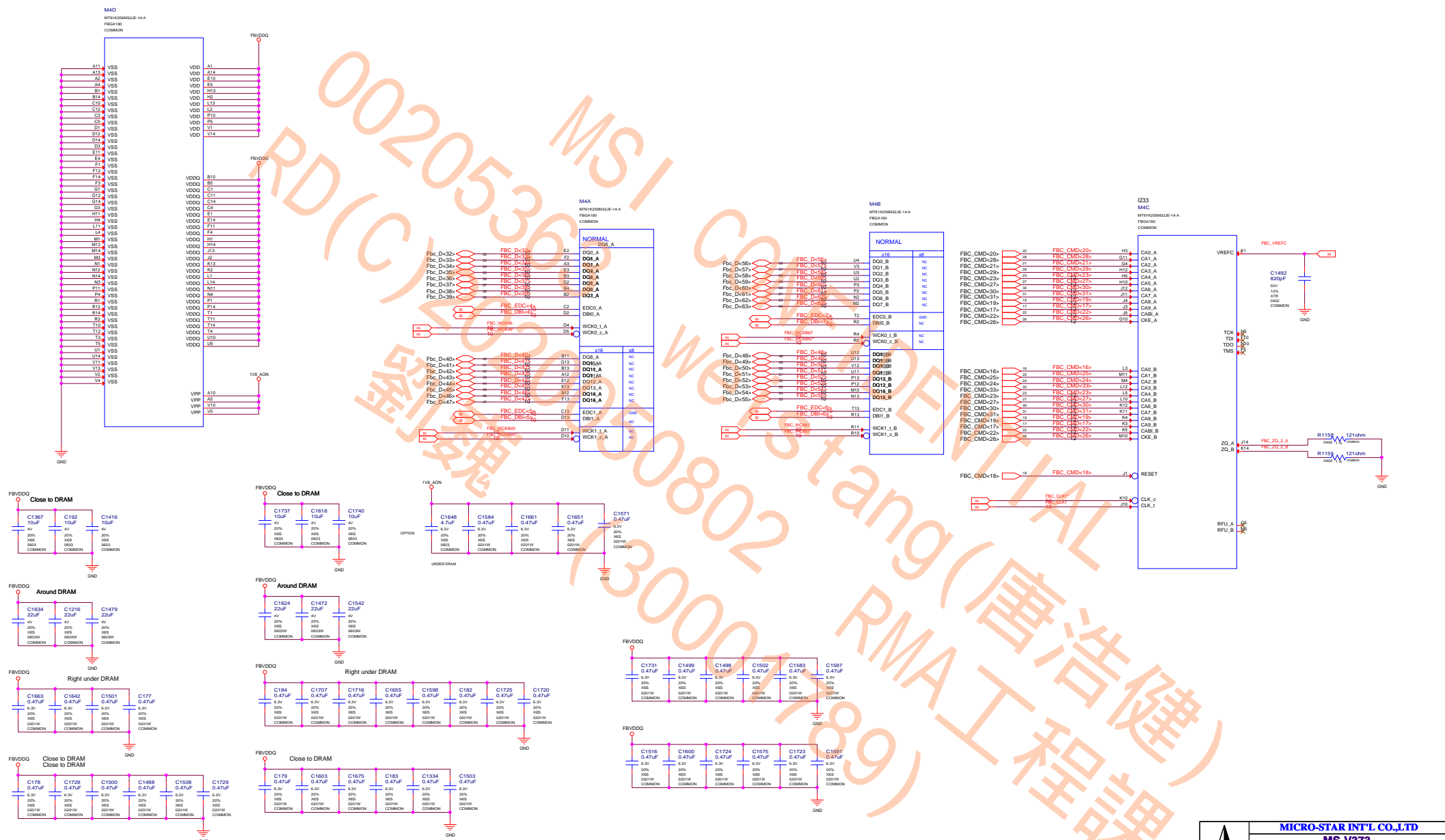


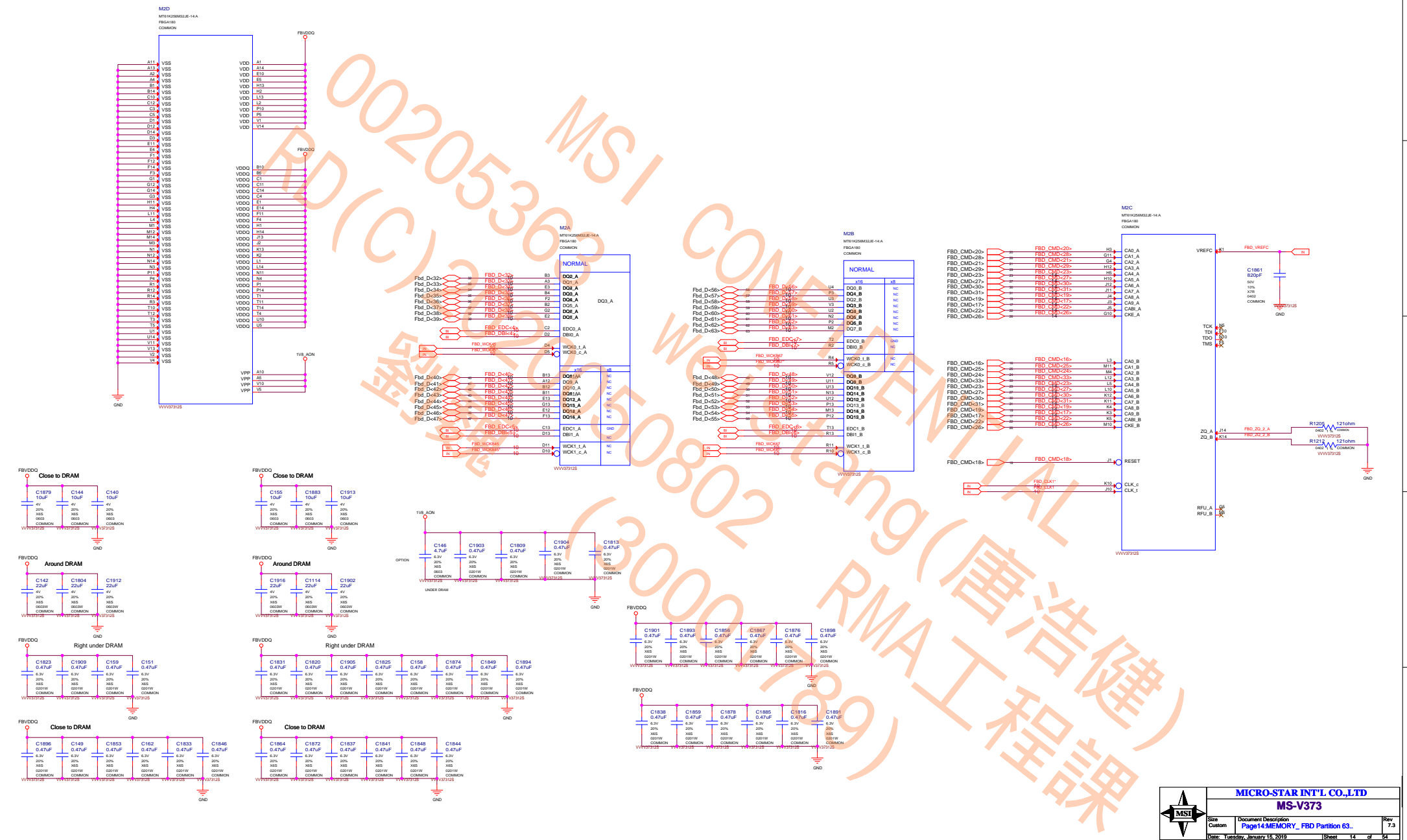


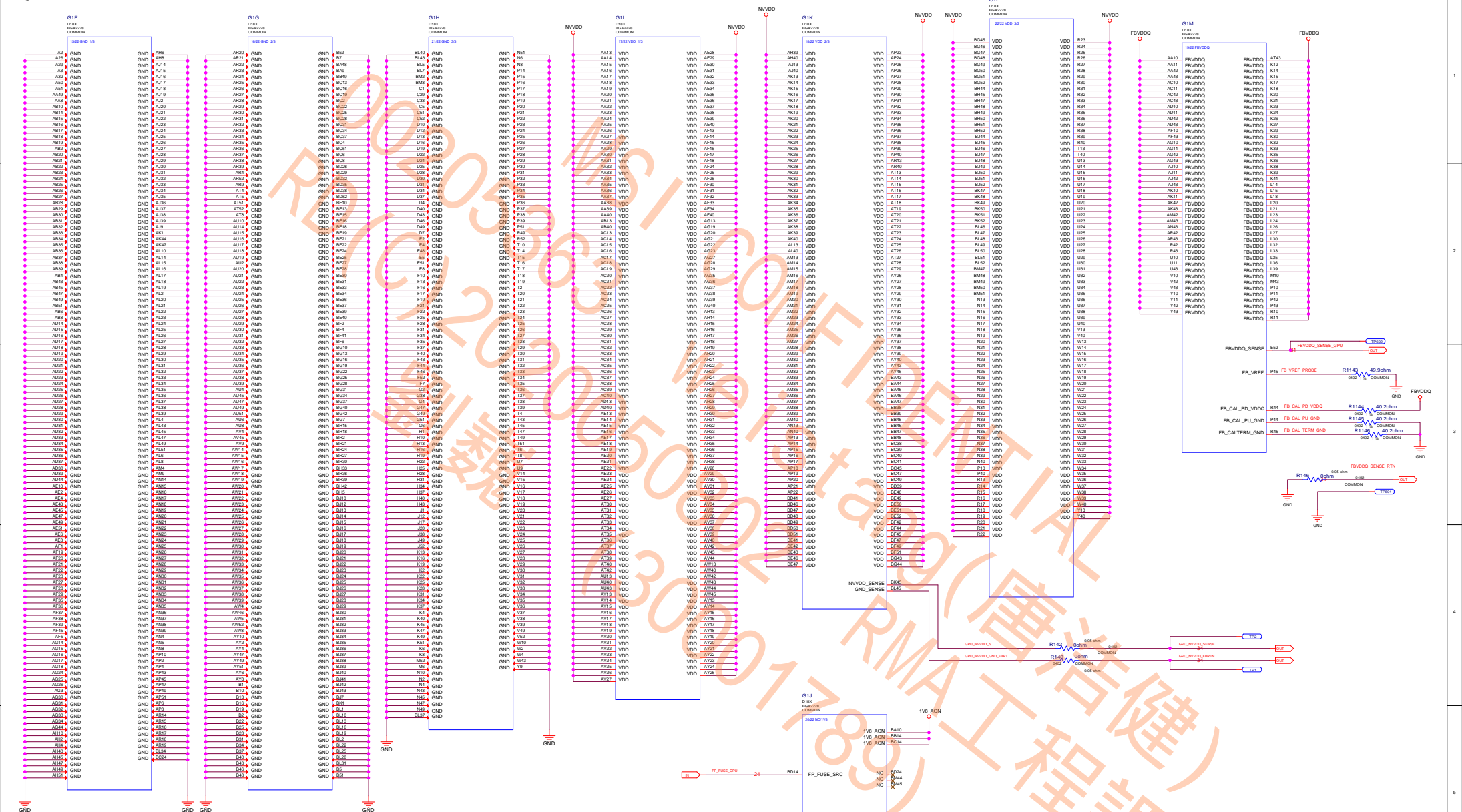








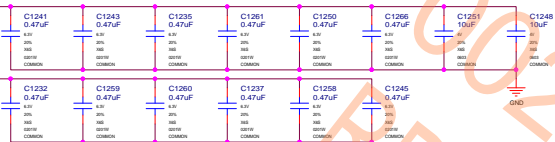




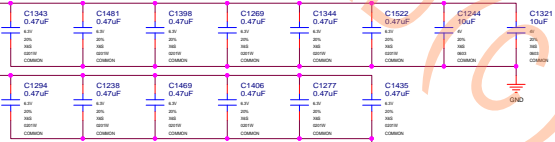
NVVDD

FBVDDQ

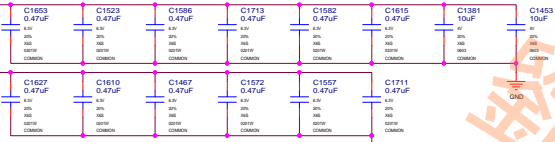
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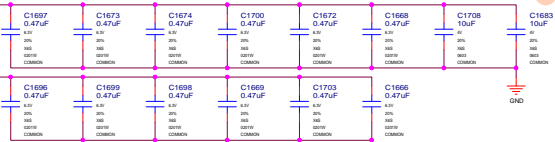
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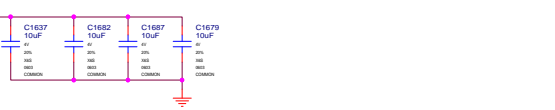
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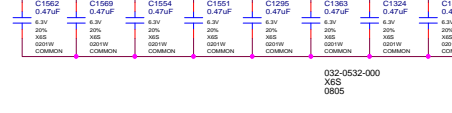
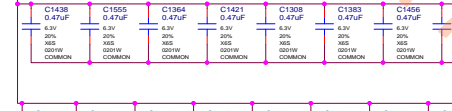
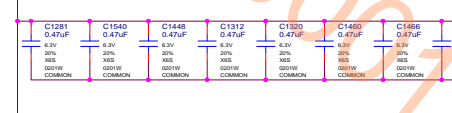
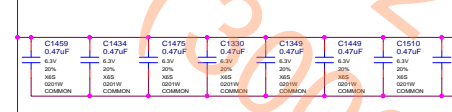
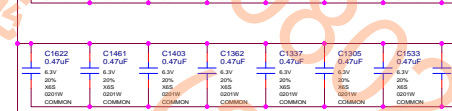
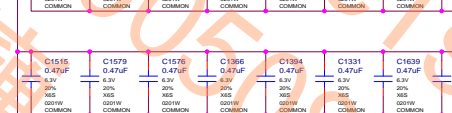
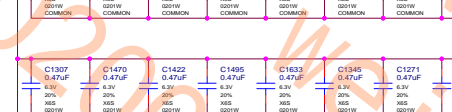
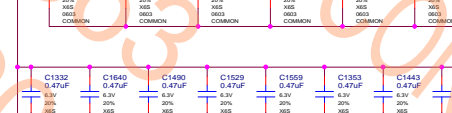
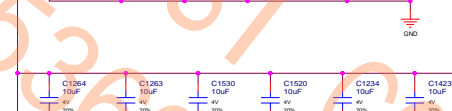
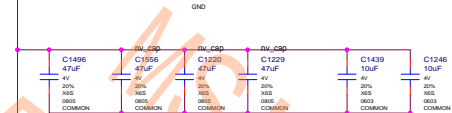
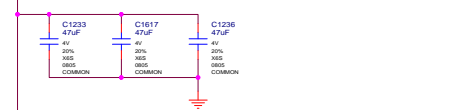
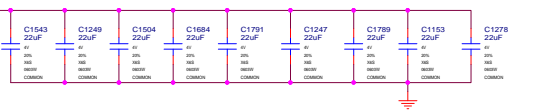
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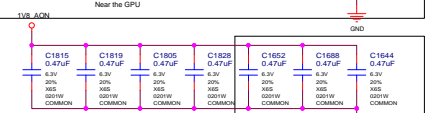
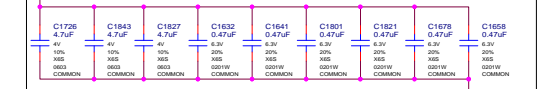
Place Close to GPU



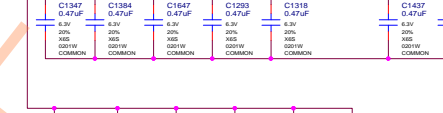
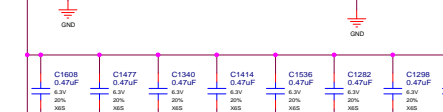
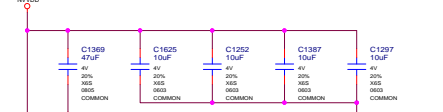
Place Close to GPU

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XES
0805

1V8_AON



NVVDD



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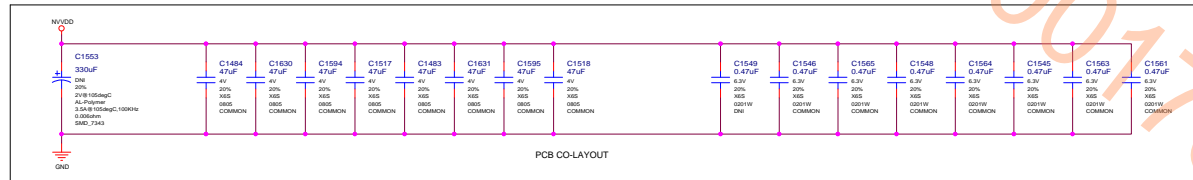
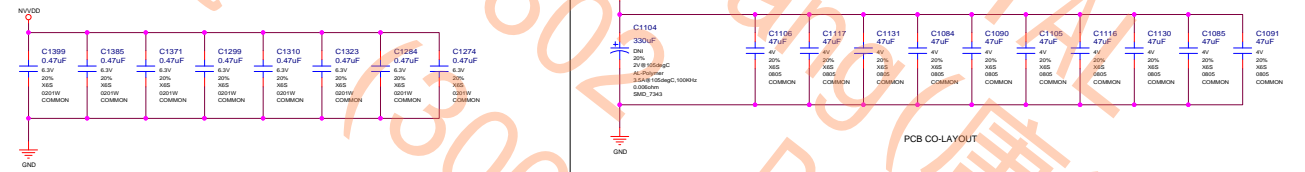
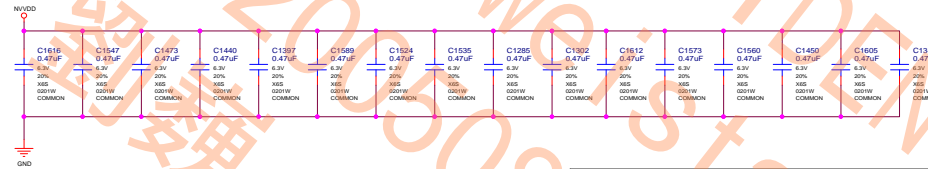
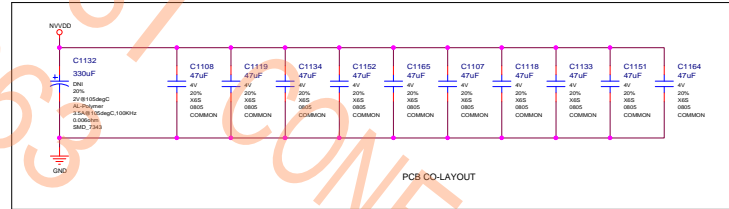
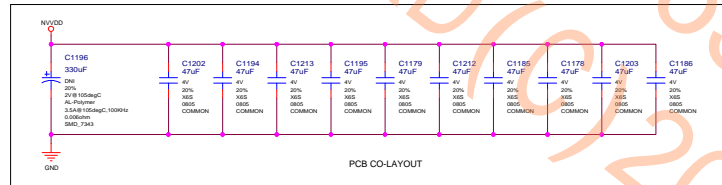
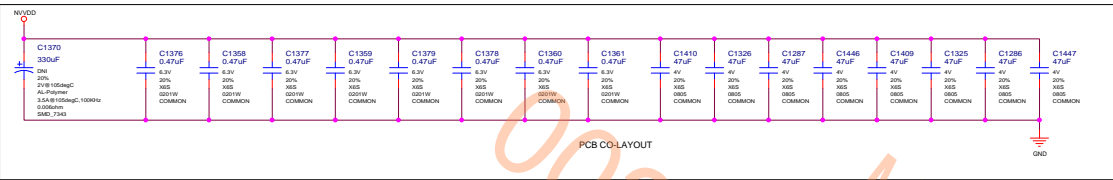
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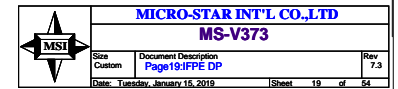
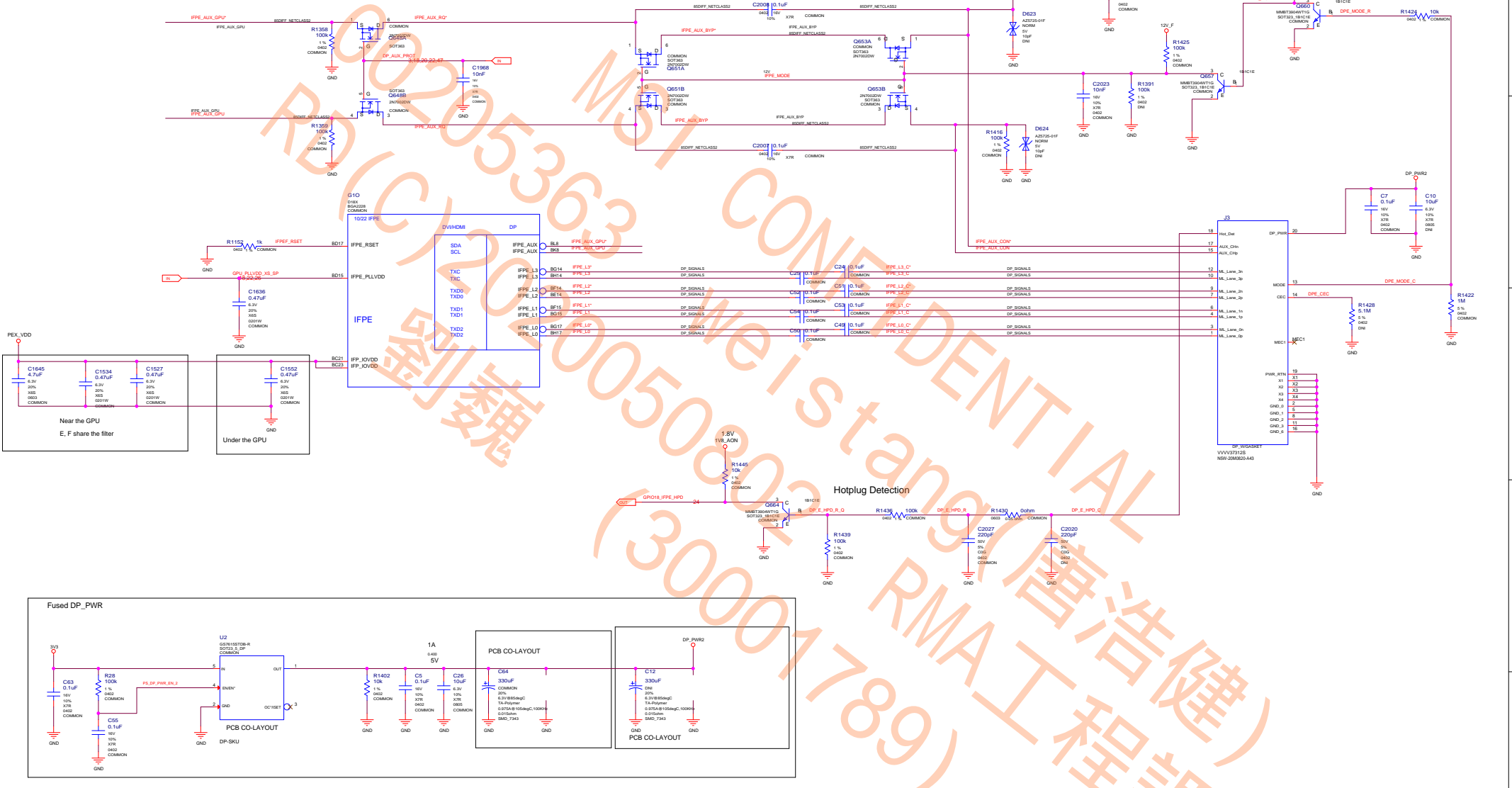
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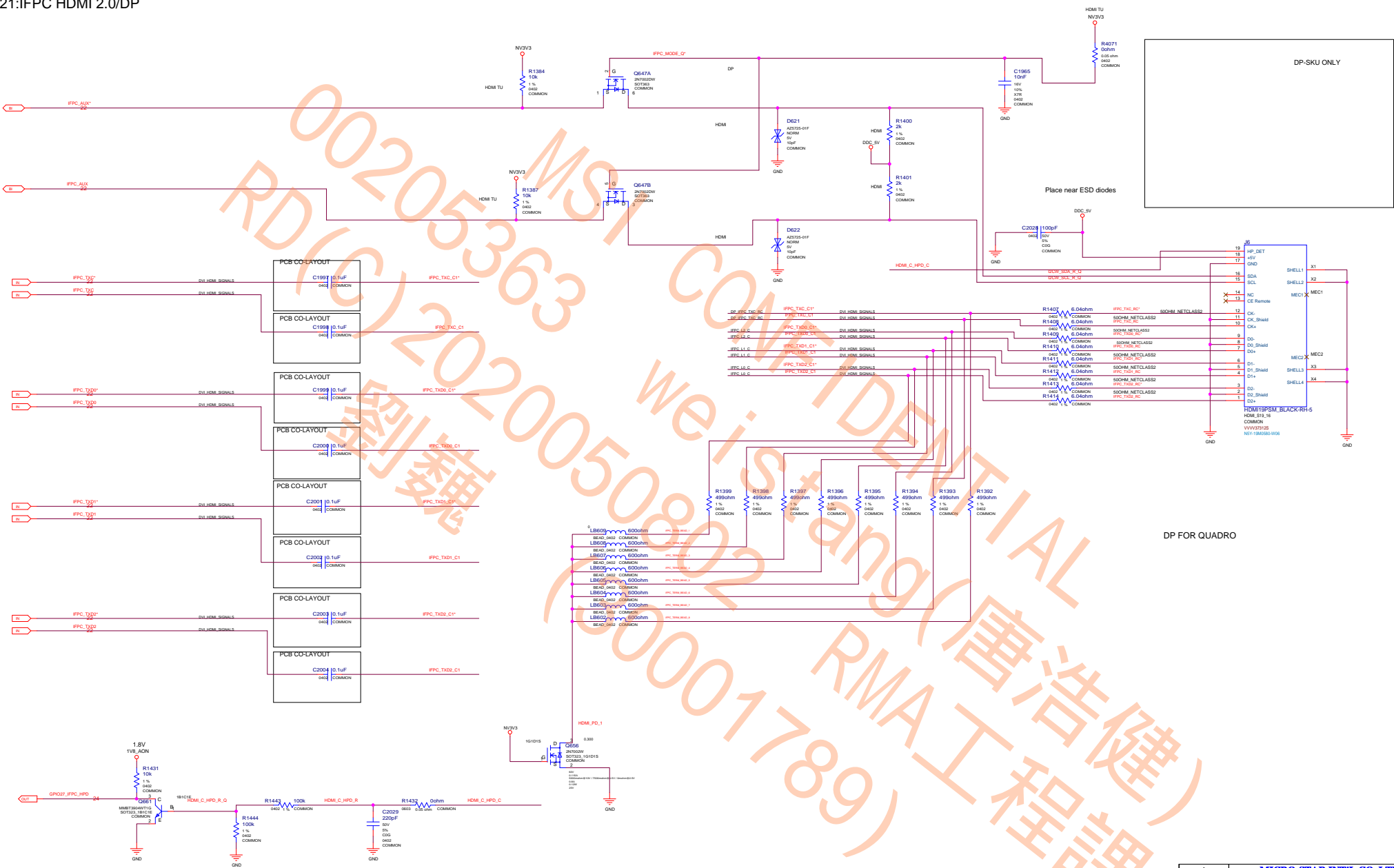
Page16:GPU Decoupling

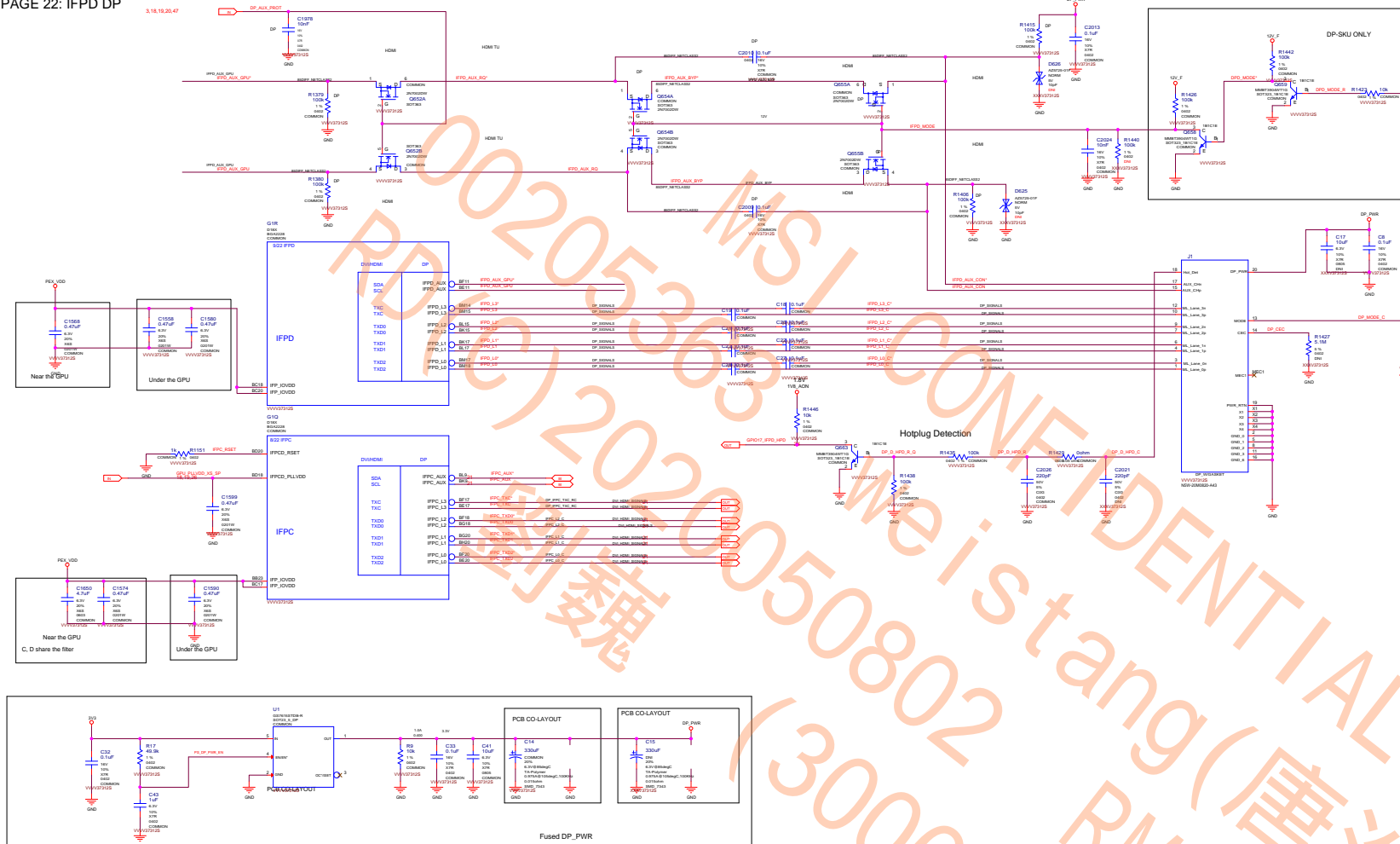
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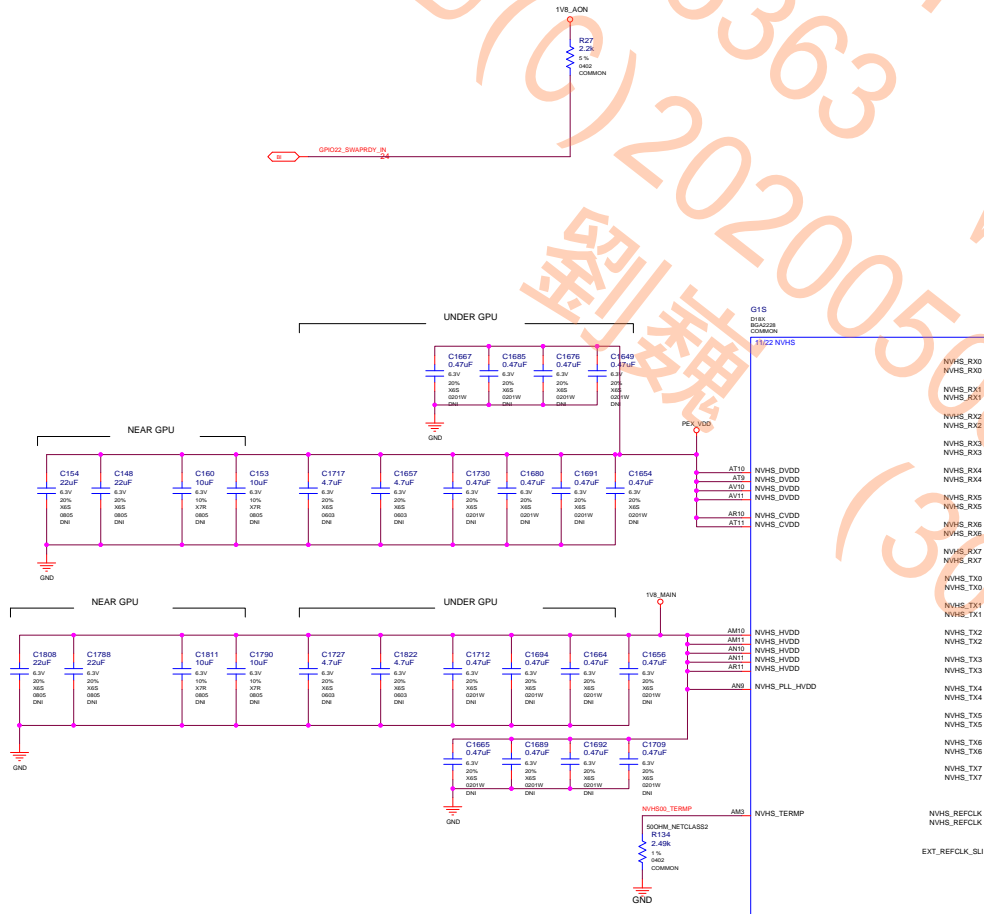
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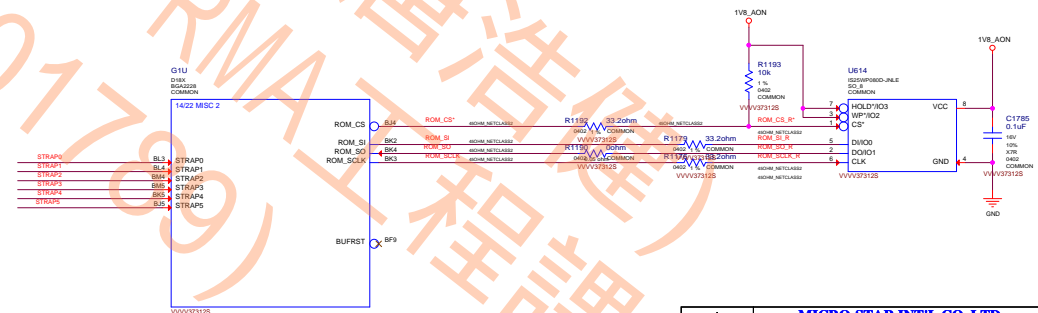
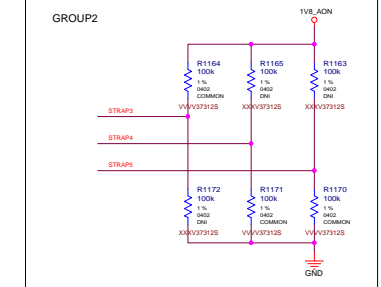
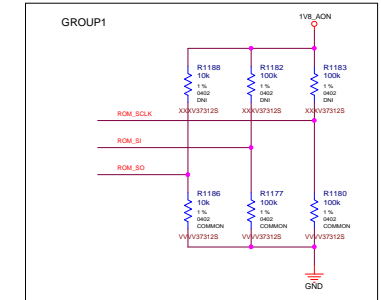
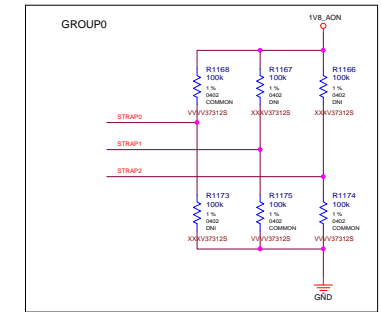
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

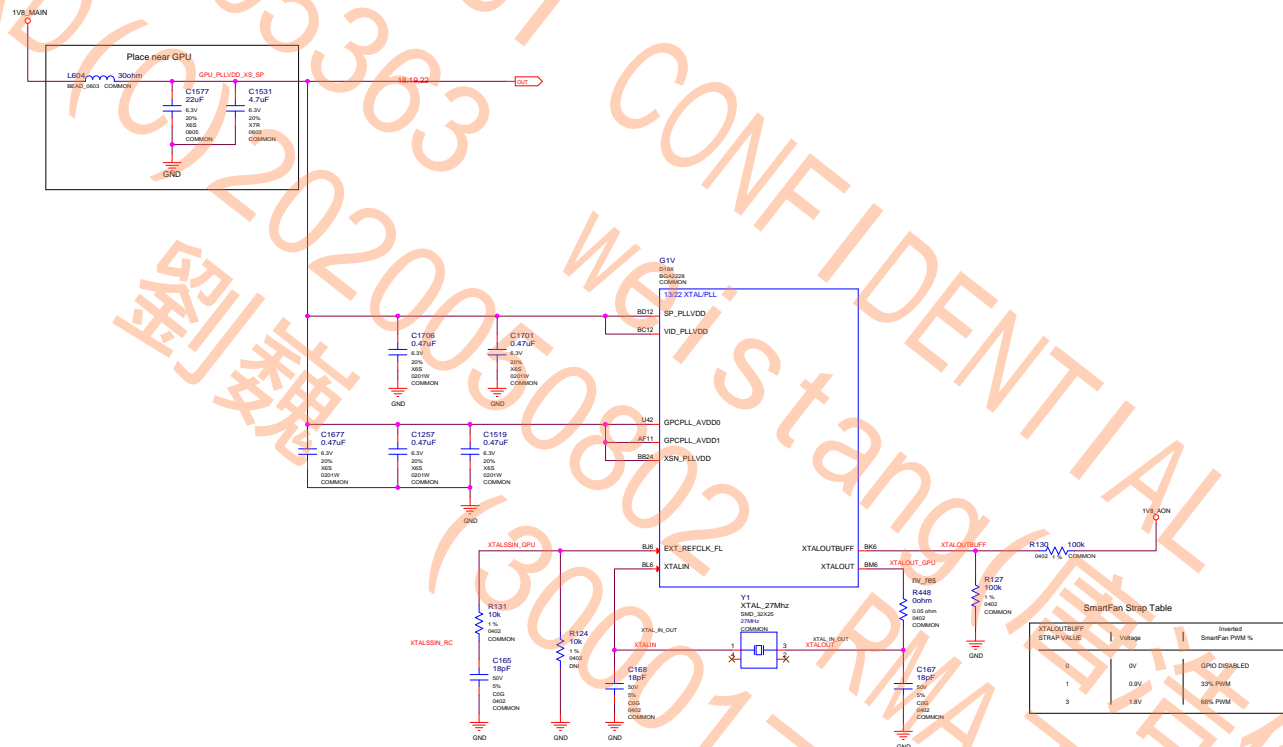
STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	RAMCFG TBD
L	L	H	0001	RAMCFG TBD
L	H	L	0010	RAMCFG TBD
L	H	H	0011	RAMCFG TBD
H	H	L	0110	RAMCFG TBD
H	H	H	0111	RAMCFG TBD

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0] FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

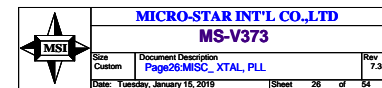
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	1:SMB_ALT_ADDR ENABLE
M	L	H	1	1	0	1	0:SMB_ALT_ADDR DISABLE
M	L	L	1	1	0	0	1:DEVID_SEL REBRAND
L	H	M	1	0	1	1	0:DEVID_SEL ORIGINAL
L	M	H	1	0	1	0	1:PCIE_CFG LOW POWER
L	M	L	1	0	0	1	0:PCIE_CFG HIGH POWER
L	L	M	1	0	0	0	1:VGA_DEVICE ENABLE
H	H	H	0	1	1	1	0:VGA_DEVICE DISABLE
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	Default
L	L	L	0	0	0	0	

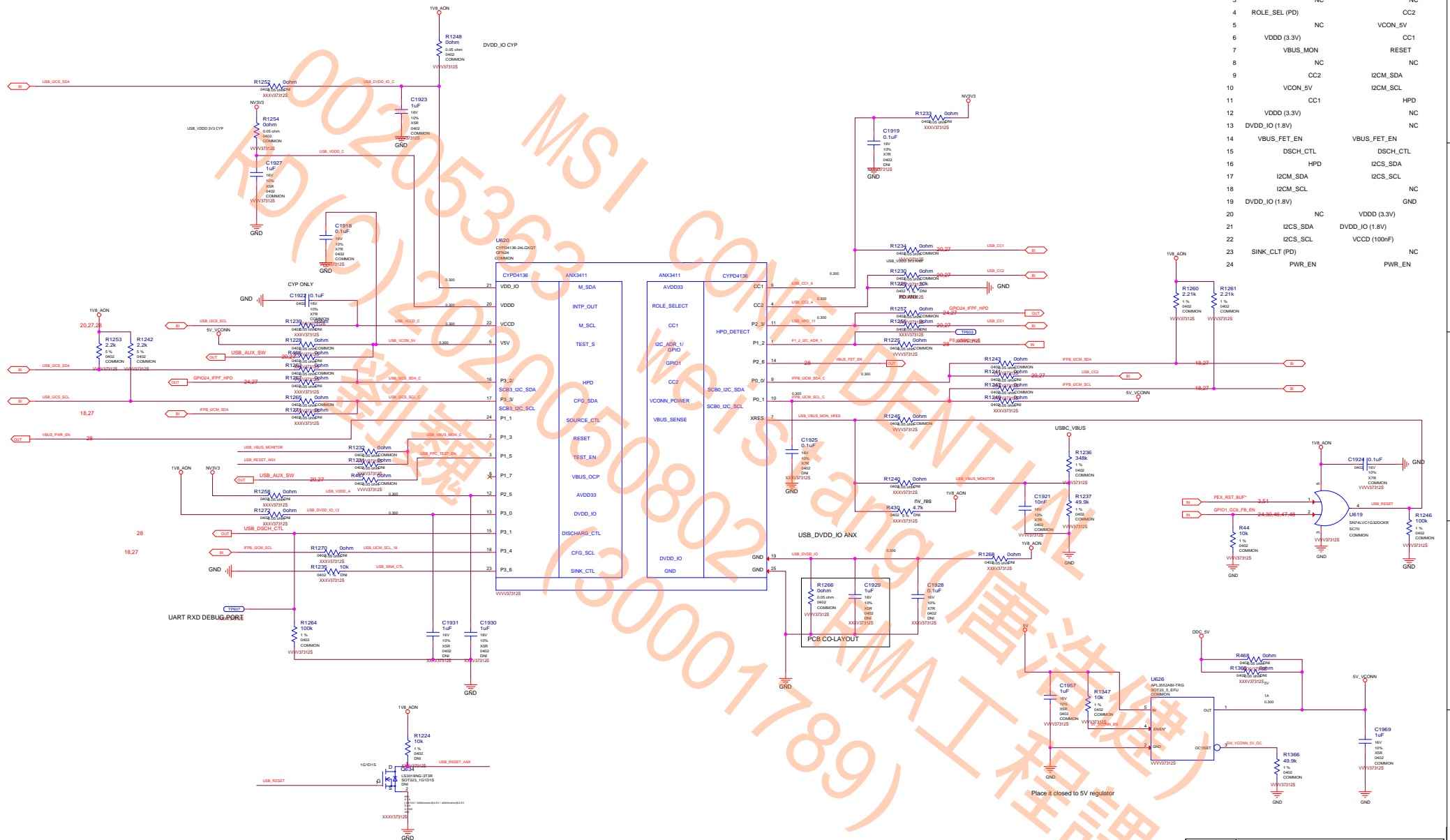
RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Samsung
00111	16Gb	256-bit	Samsung



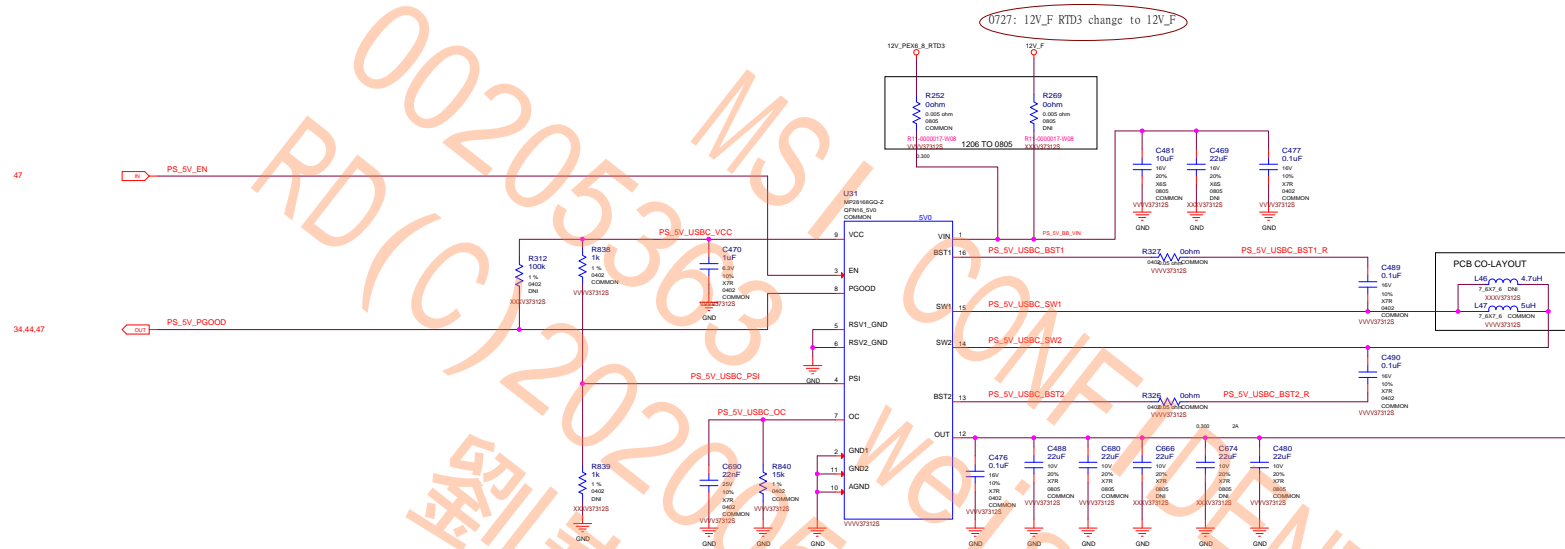


XTALOUTBUFF STRAP VALUE	Voltage	Inverted SmartFan PWM %
0	0V	GPIO DISABLED
1	0.9V	33% PWM
3	1.8V	66% PWM



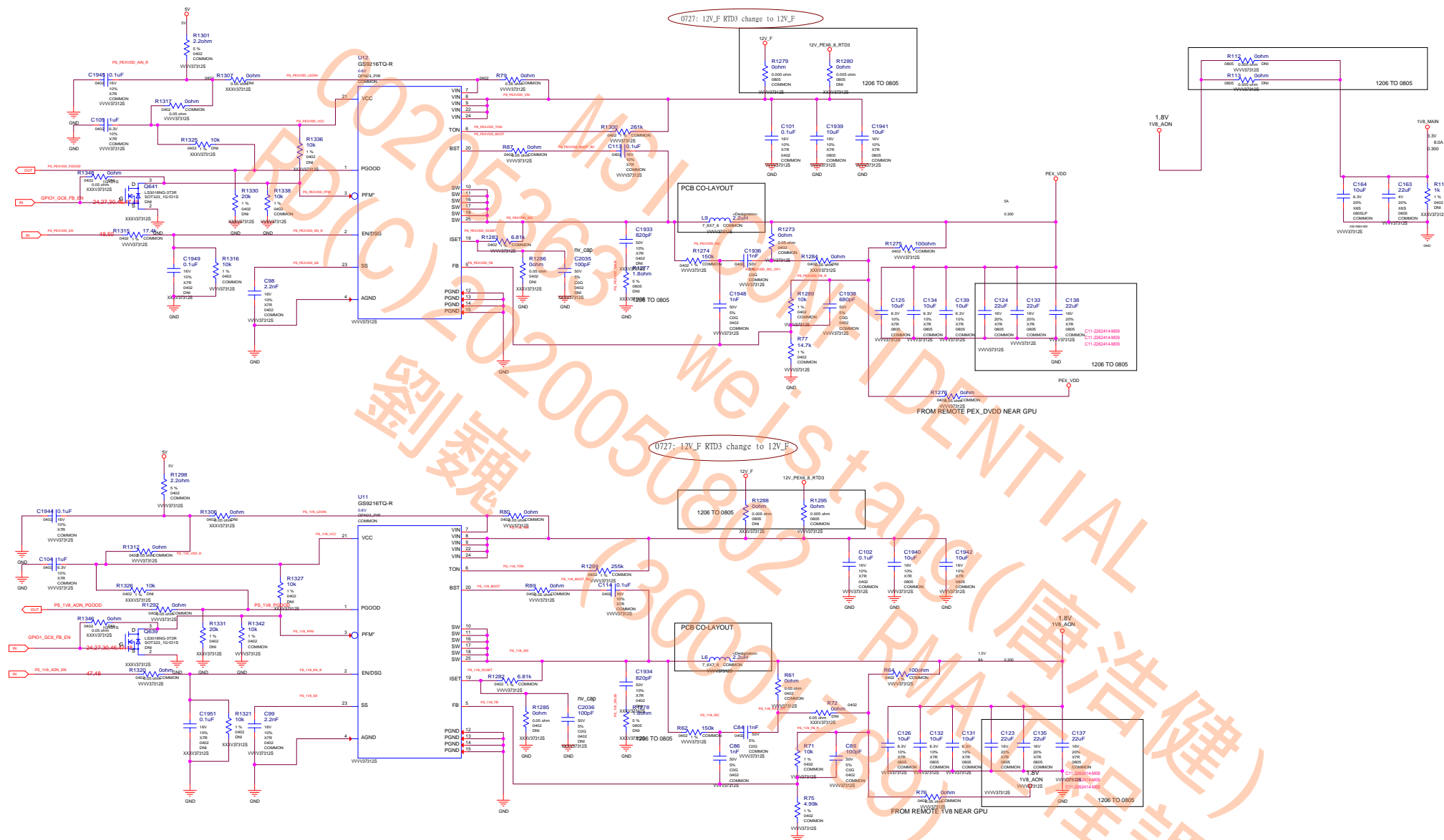


PIN	ANX	CYP
1	TP	
2	RESET	VBUS_MON
3	NC	NC
4	ROLE_SEL (PD)	CC2
5	NC	VCON_5V
6	VDDD (3.3V)	CC1
7	VBUS_MON	RESET
8	NC	NC
9	CC2	I2CM_SDA
10	VCON_5V	I2CM_SCL
11	CC1	HPD
12	VDDD (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDD (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCCD (100kF)
23	SINK_CLT (PD)	NC
24	PWR_EN	PWR_EN



remove





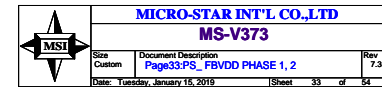
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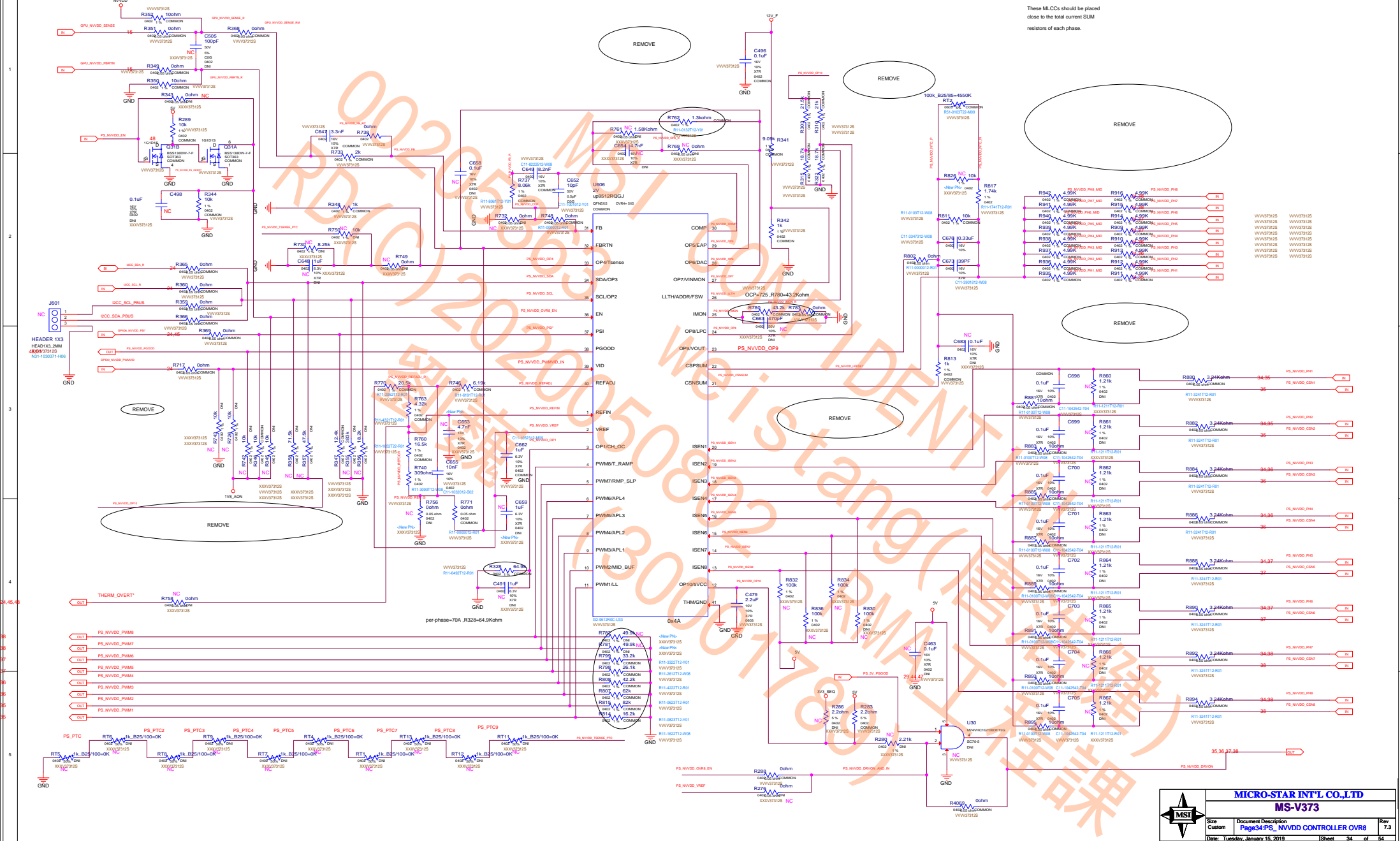
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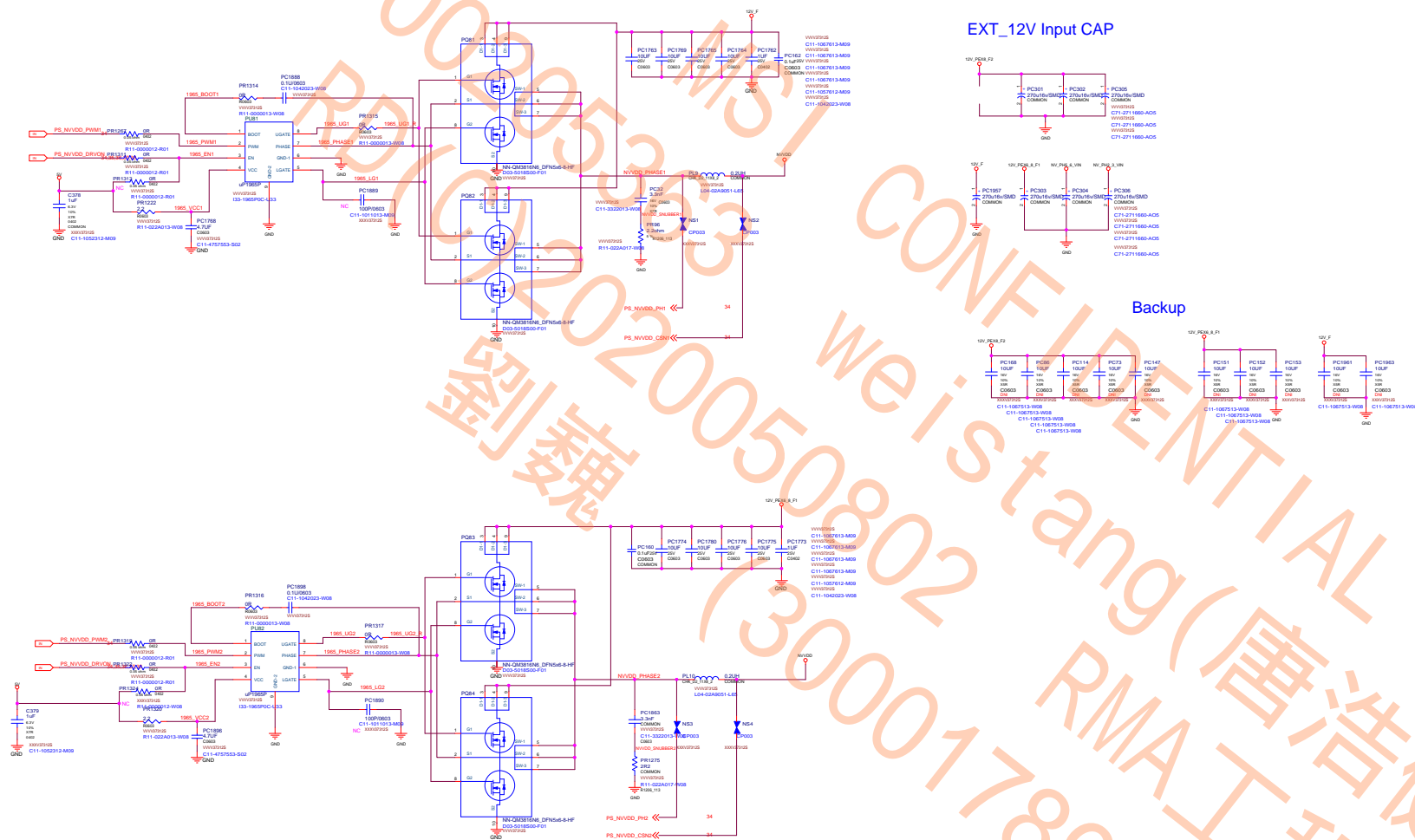
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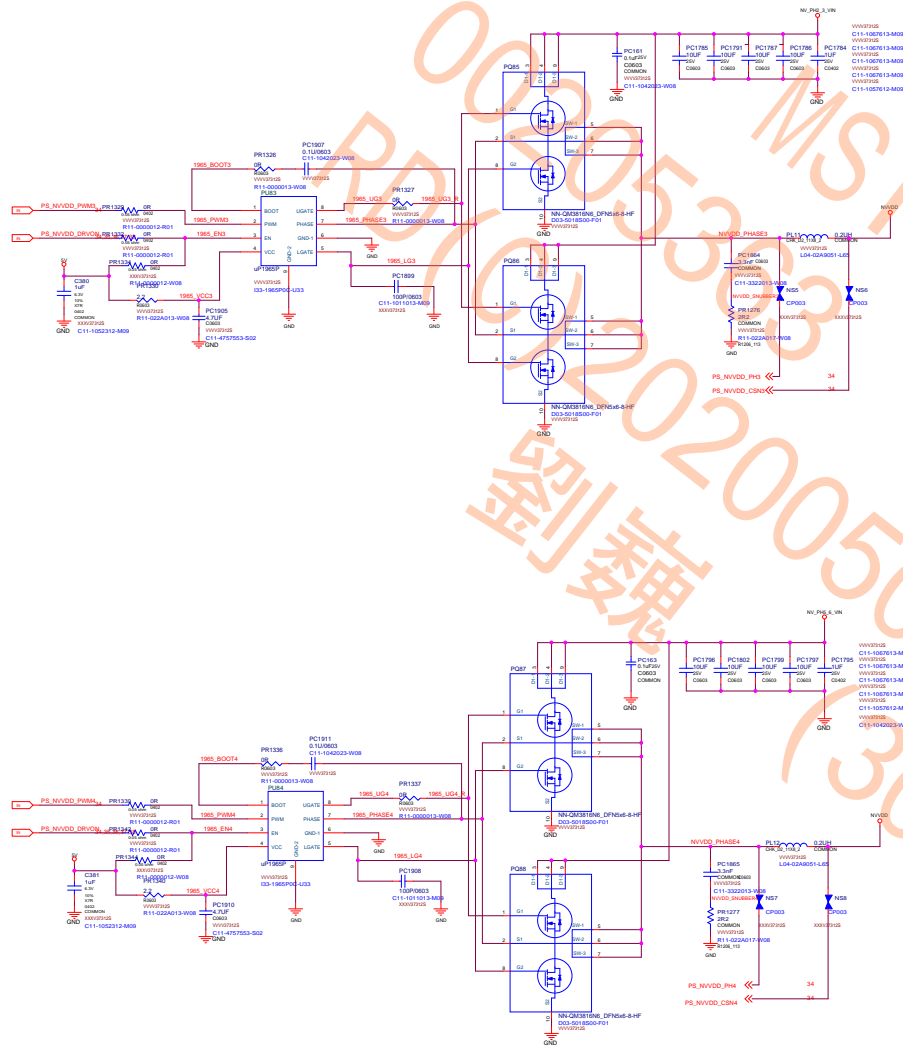
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weistang (唐浩健)
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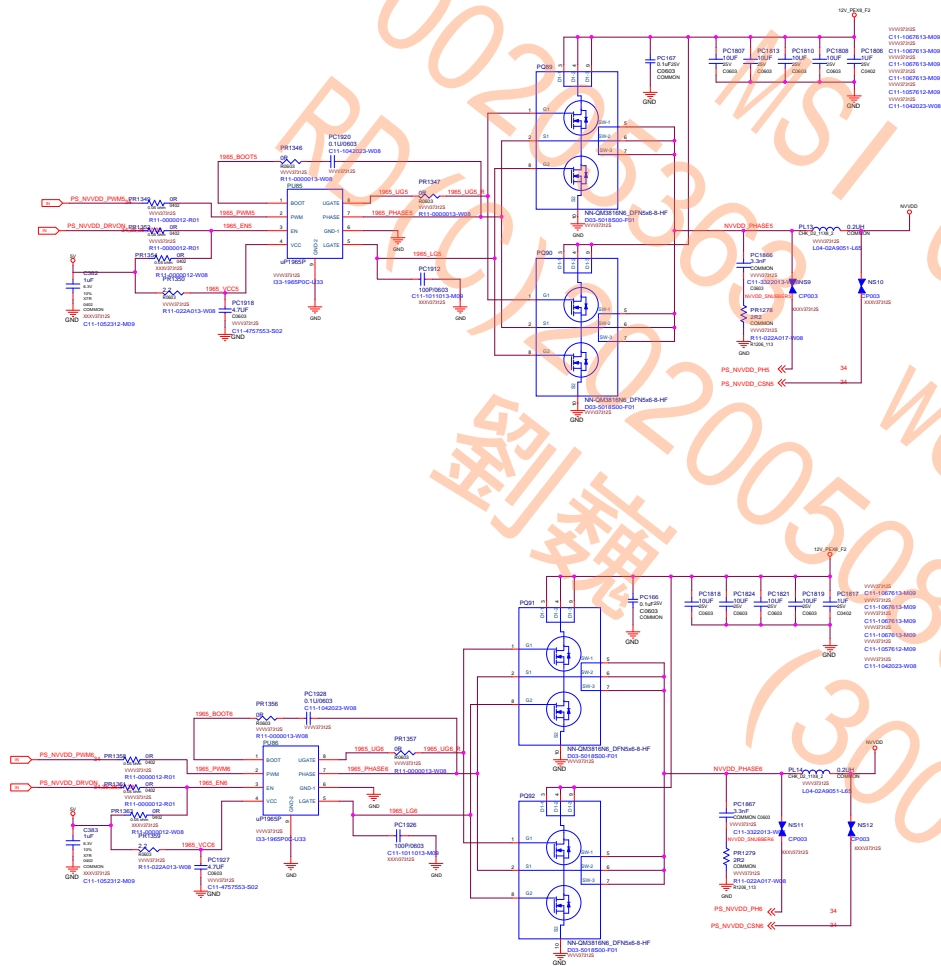
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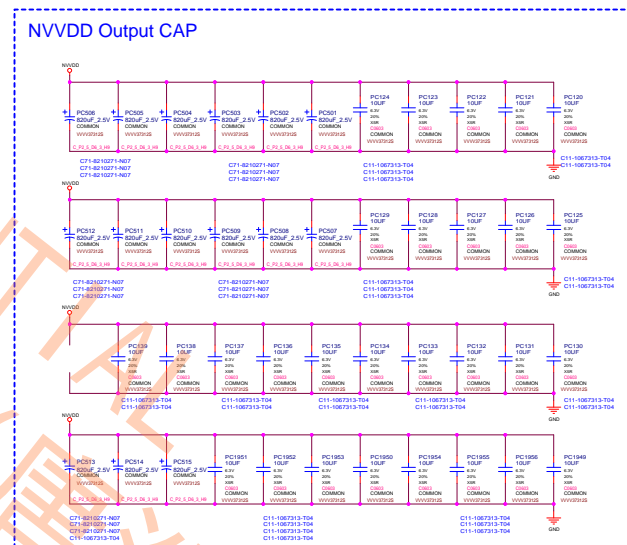
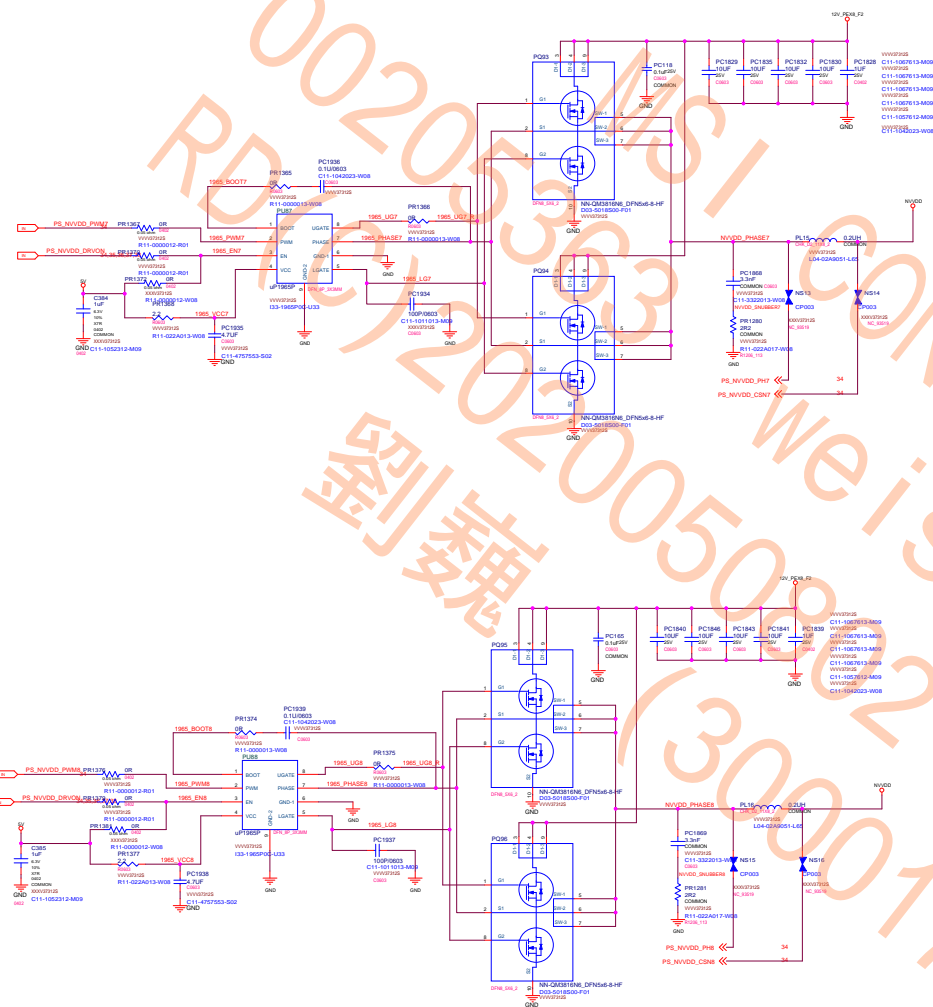








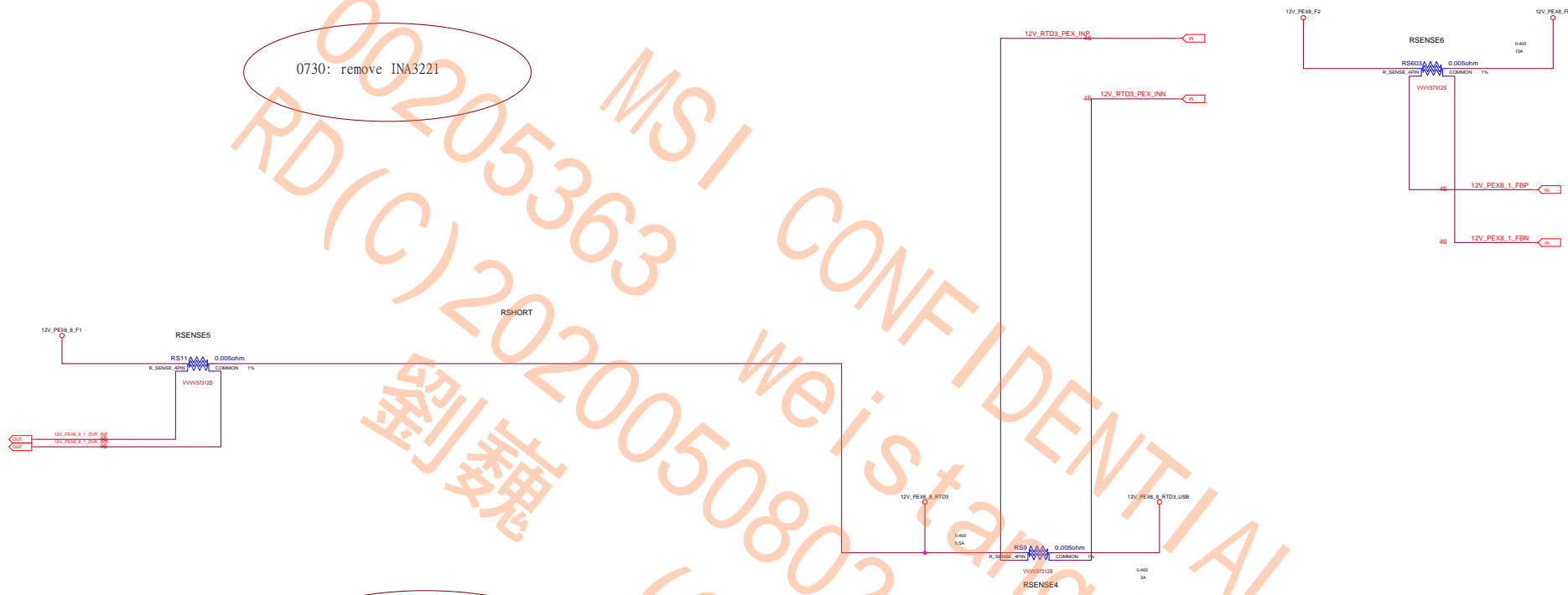


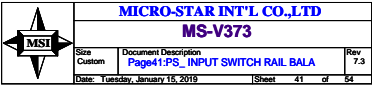


AND GATE LOGIC FOR P-BOARD			
GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

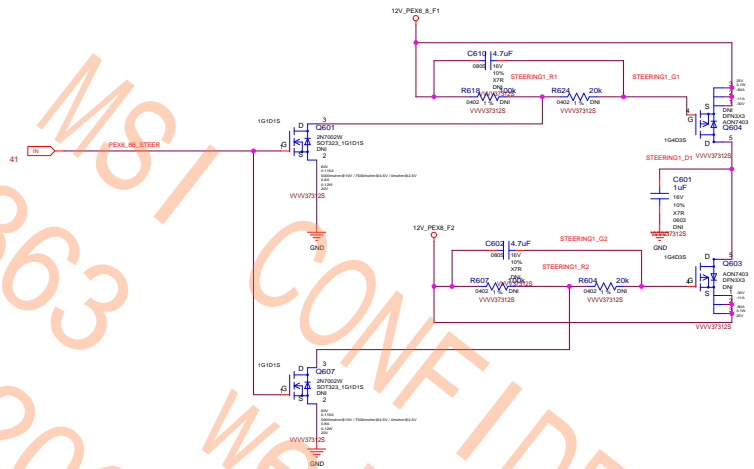
AND GATE LOGIC FOR P-BOARD			
GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A

0727: remove

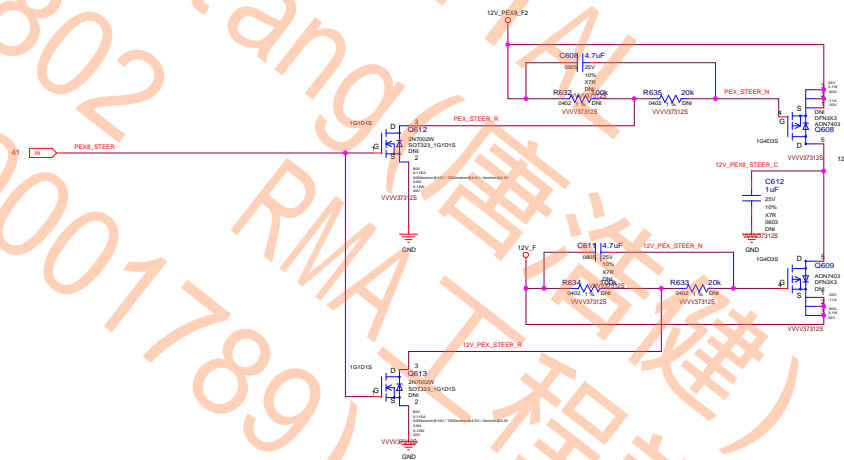




12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA

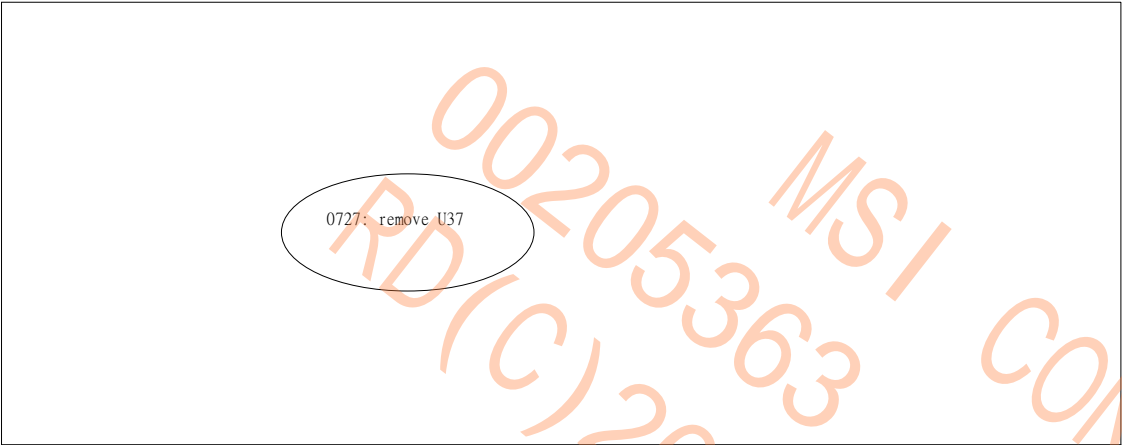


12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

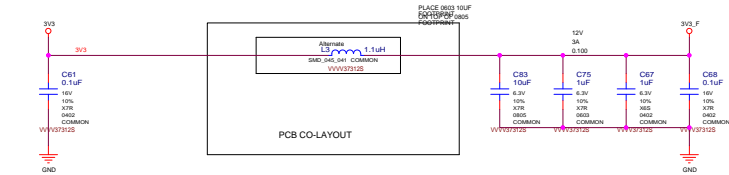


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劉魏
weistang(唐浩健)
(30001789)
RMA工程課

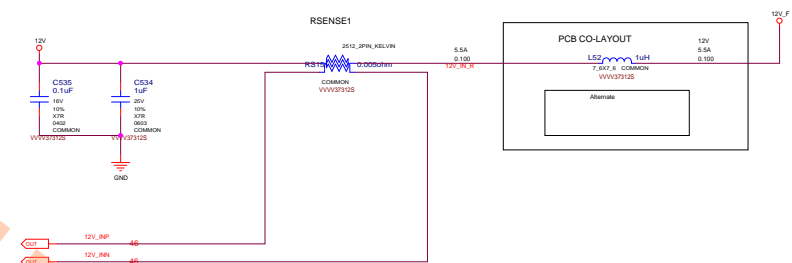
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MS-V373		
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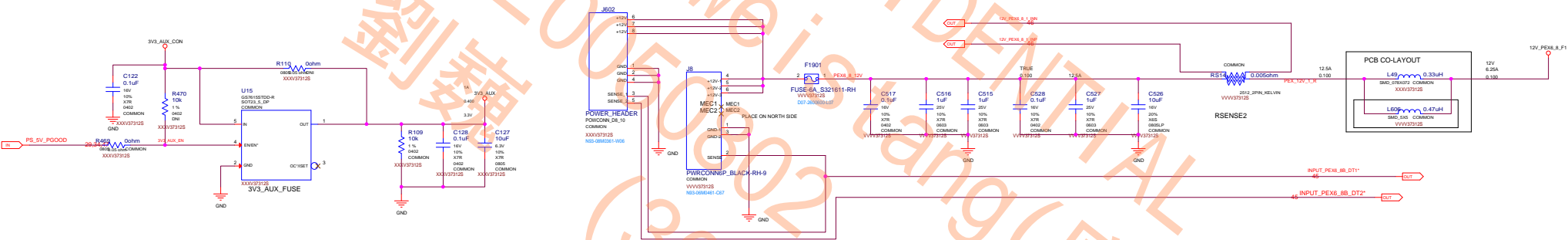
PEX 3V3 INPUT - 10W



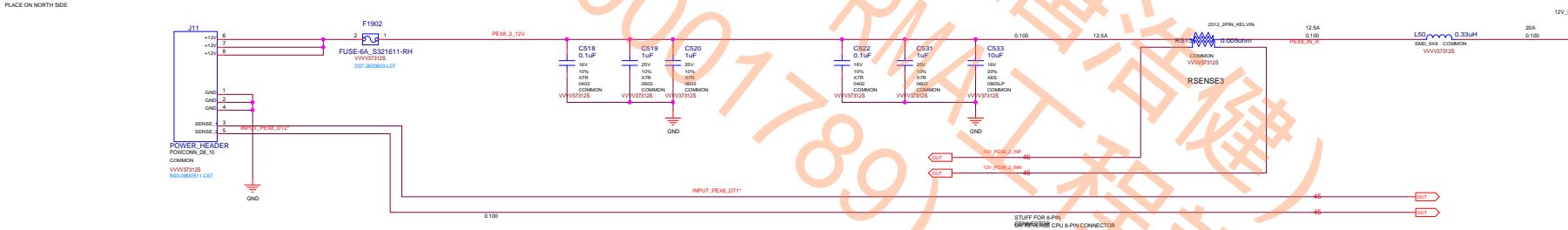
PEX_12V INPUT - 66W

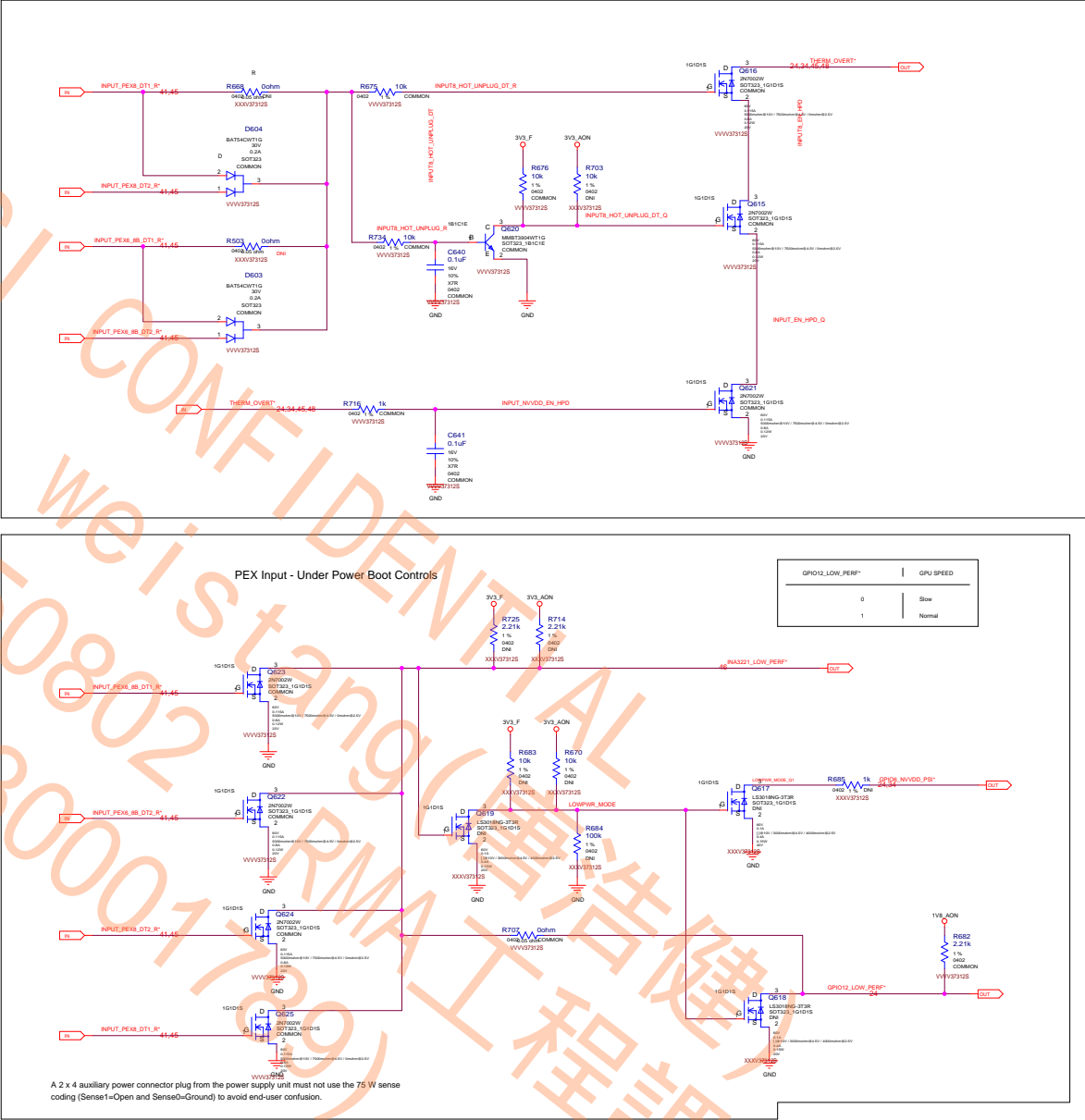
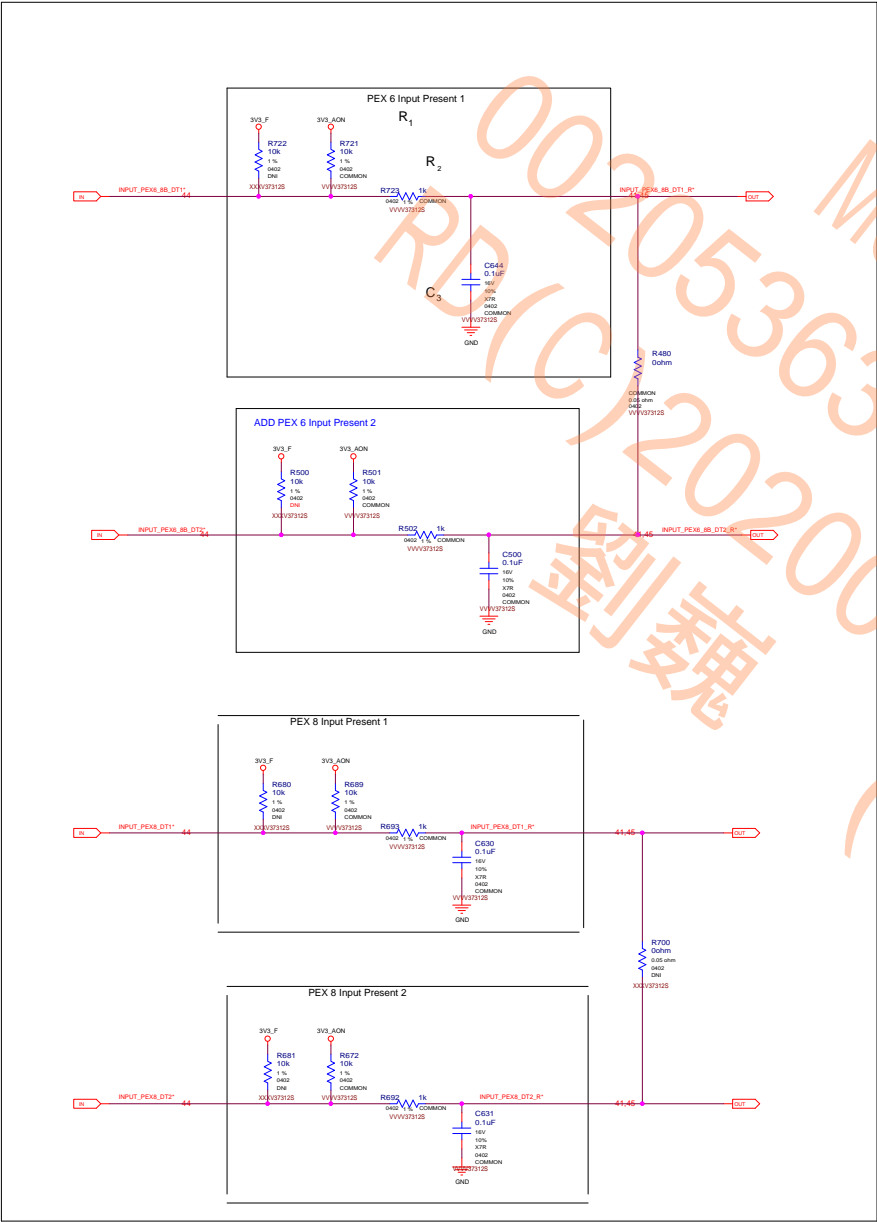


PEX6 INPUT 1 - 2x3 PCIE CON 75W

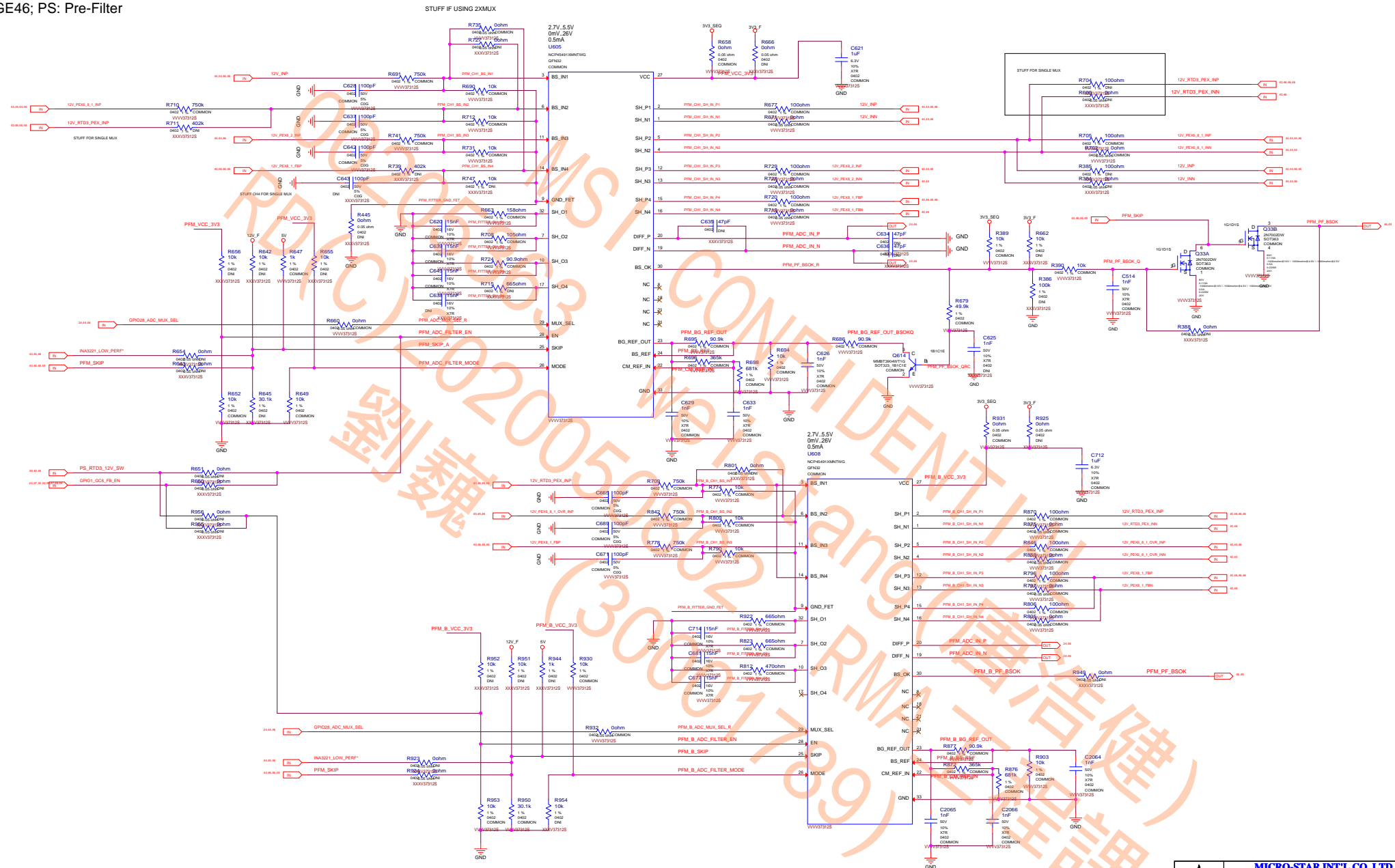


PEX8 INPUT 2 - 2x4 PCIE CON 150W



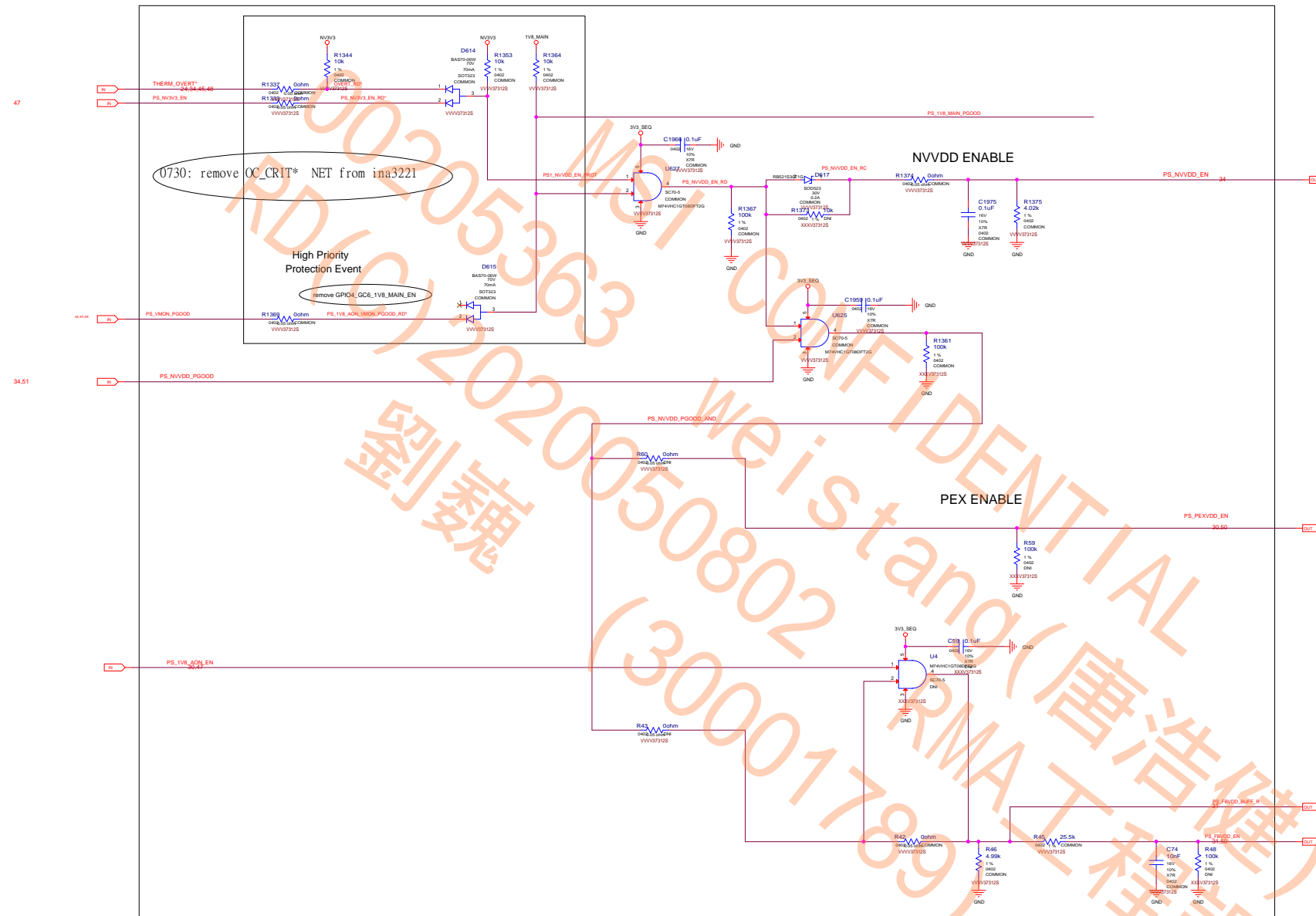


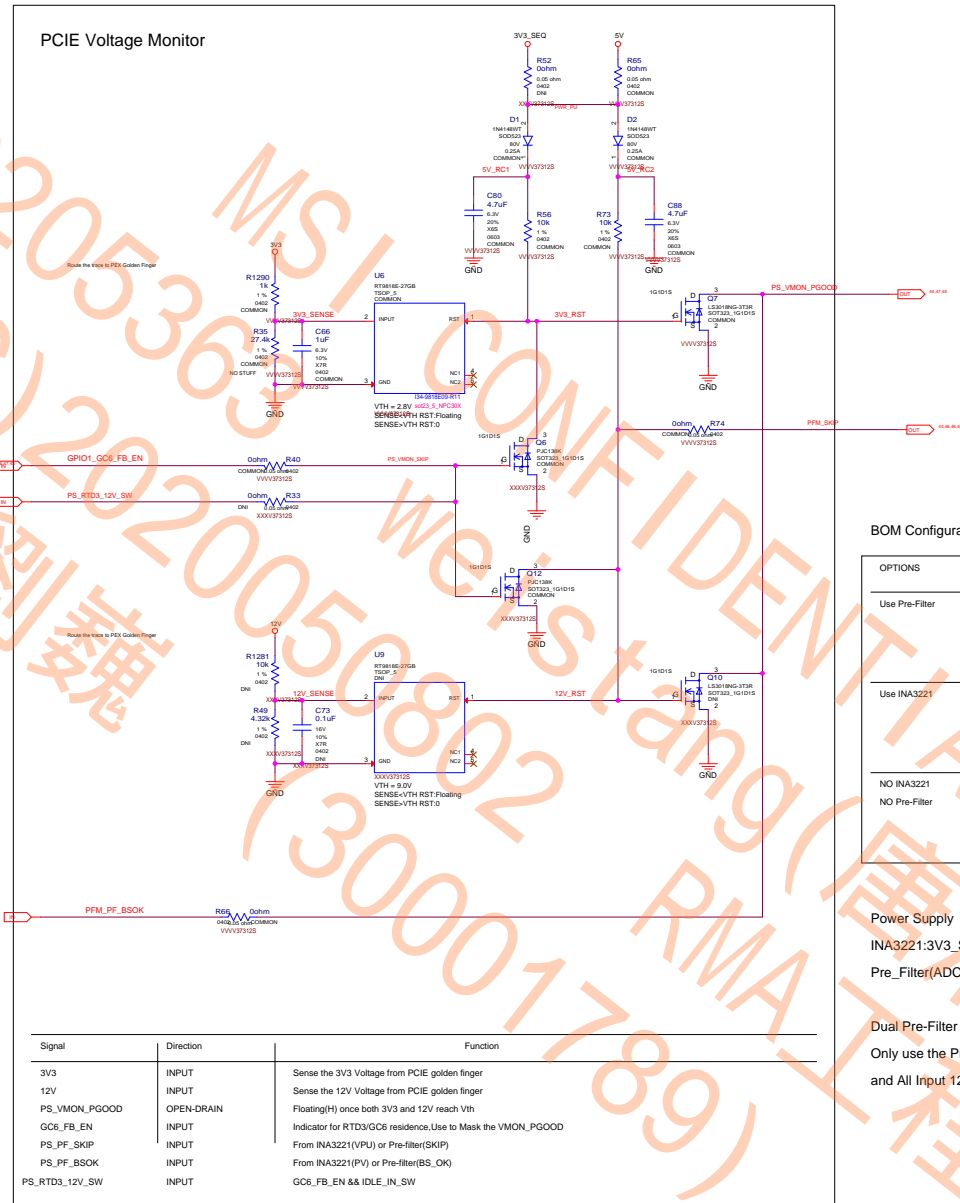
GPI012_LOW_PERP*	GPIU SPEED
0	Slow
1	Normal



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BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

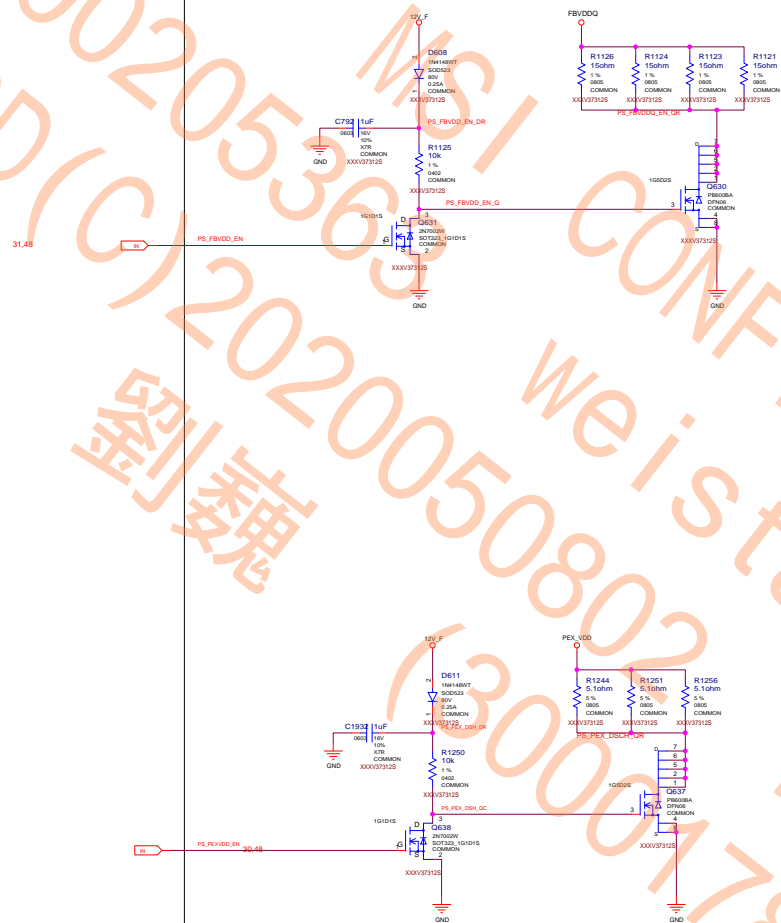
Power Supply

INA3221:3V3_SEQ

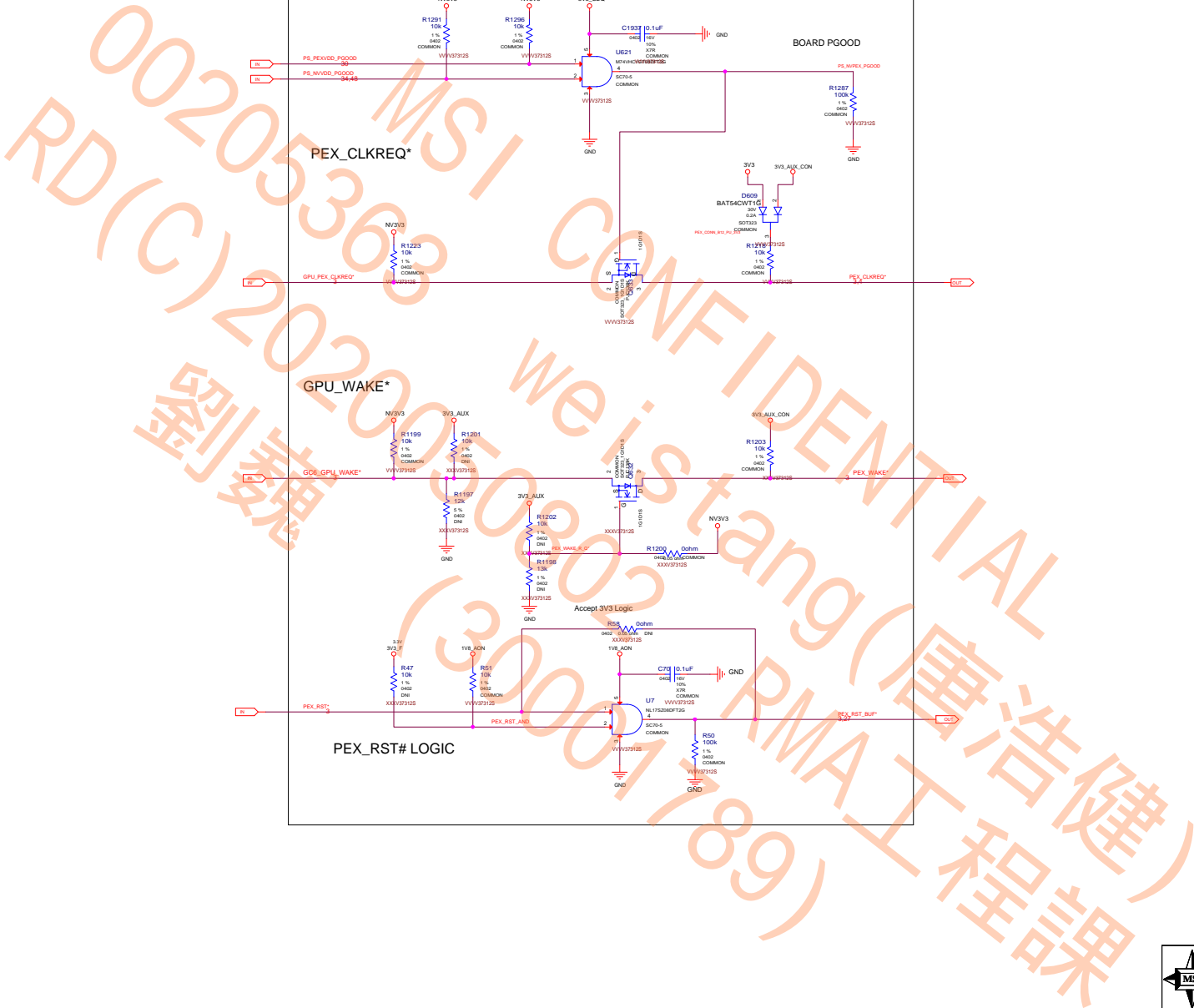
Pre_Filter(ADC_MUX):3V3(PEX)

Dual Pre-Filter case:

Only use the Primary Pre-Filter to sense 3V3PEX
and All Input 12Vs



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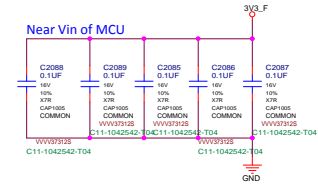
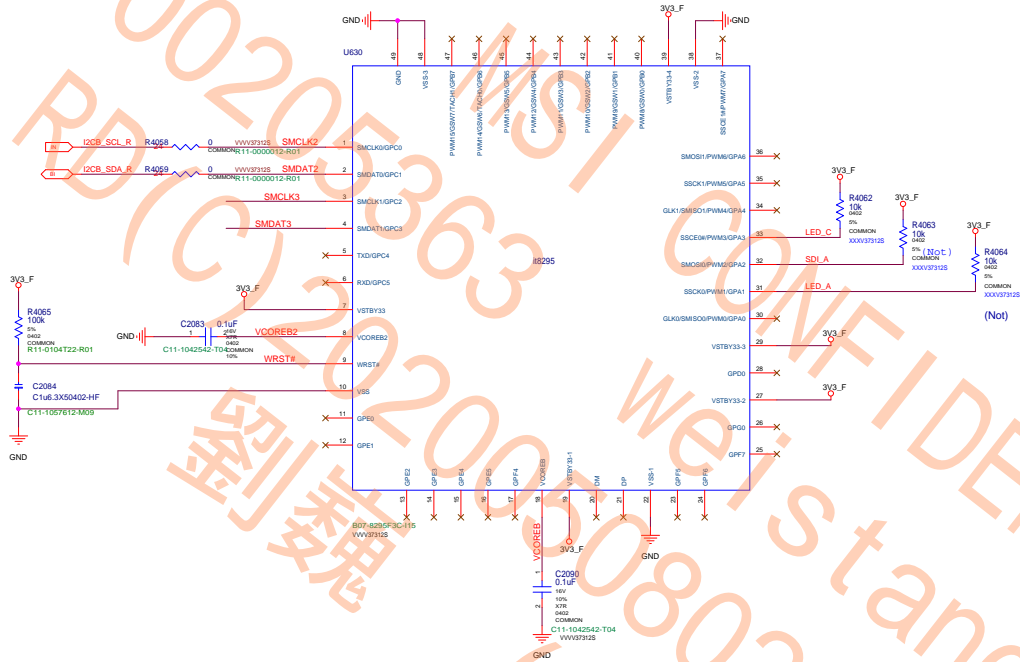
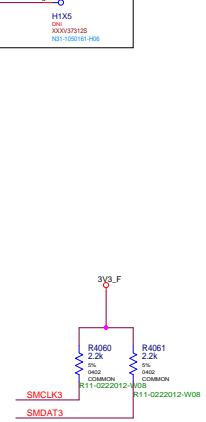
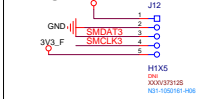


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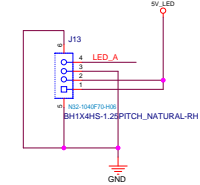
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Firmware Programming

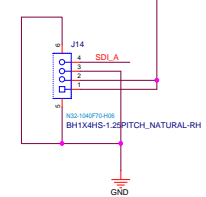
Debug



LED_A



LED_B



5V_LED

